

SLUS644B – FEBRUARY 2005 – MAY 2005

DUAL SLOT PCI-X 2.0 HOT-PLUG POWER CONTROLLER

FEATURES

- Supports PCI, PCI−X 1.0 and PCI−X 2.0 Slots
- Internal Power Switches for −12 V, 12 V, 3.3 V Aux
- Control for Power FETs for 5 V, 3.3 V, and VIO
- Overload Protection on All Supplies
- Current Regulation on 3.3 V, 5 V and VIO Supplies
- Soft Start to Minimize Inrush Current
- Programmable Slew Rate for 3.3 V, 5 V, 12 V, VIO and Vaux Supplies
- Direct Control of All Functions
- VIO Selection Based on Card Type
- 80-Lead PowerPad™ HTSSOP Package
- Narrow Package that Fits Between PCI Slots

APPLICATIONS

- Hot Plug Slots in Servers

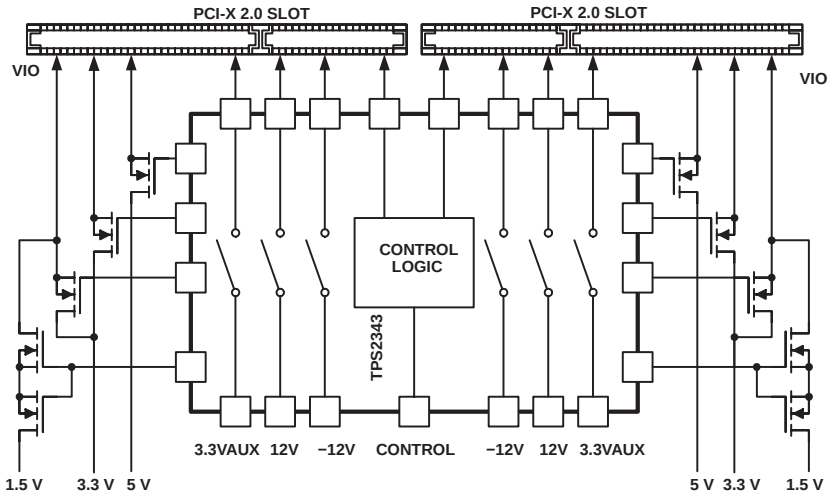
DESCRIPTION

Each TPS2343 contains main supply power control, auxiliary supply power control, power FETs for 12-V, −12-V and auxiliary 3.3-V supplies, VIO control, and digital control for two slots.

The main power control circuits start with all supplies off and all outputs are held off until PGOOD is asserted, indicating that system supplies are valid. Then, when power enable is asserted, the control circuit applies constant current to the gates of the power FETs, allowing each FET to ramp load voltage linearly. Each supply can be programmed for a desired ramp rate by selecting the appropriate gate capacitor. The TPS2343 monitors load current and regulates peak current to prevent disturbances to the system power rails. If load current remains regulated for longer than 5 ms, that slot is latched off.

Logic inputs to the TPS2343 access all functions of the TPS2343. All status information from the TPS2343 is available on logic outputs.

SIMPLIFIED APPLICATION DIAGRAM



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DESCRIPTION (CONT.)

Auxiliary power control circuits switch, ramp, and monitor 3.3-V auxiliary power to each slot and control data switches that connect slot power management event (PME) outputs to the main PME bus after auxiliary supply is ramped. PME is disconnected when a board is turned off or a fault occurs on the board's auxiliary power. A fault on auxiliary power also shuts off main power to that board.

VIO control consists of gate drivers to select between 3.3 V and 1.5 V in response to command and current limiting circuitry to shut down a slot in the event of over current. Each TPS2343 contains power FETs for 12 V, −12 V, and auxiliary 3.3 V for two slots. These power FETs are short-circuit protected, slew rate controlled, and over-temperature protected.

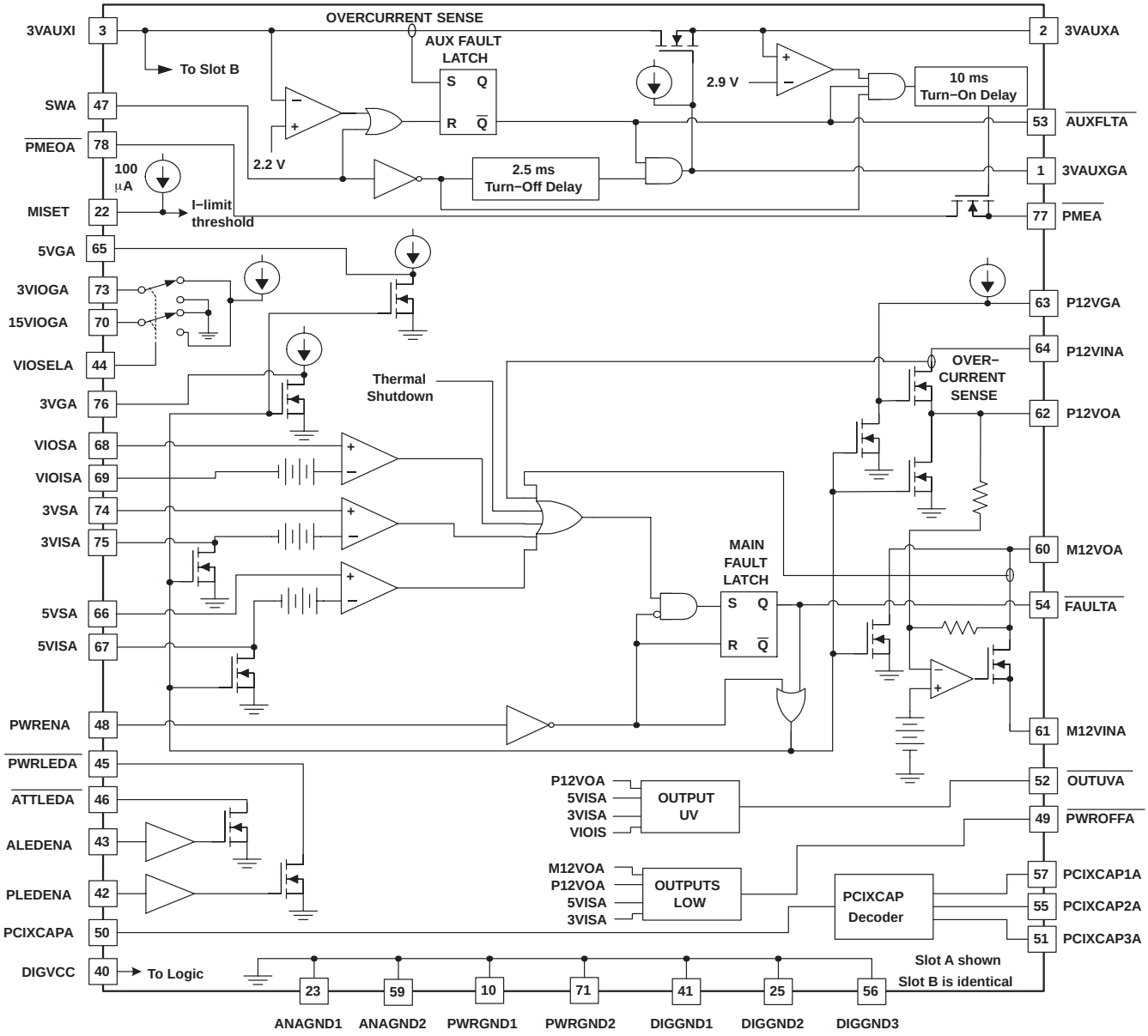
The TPS2343 includes novel current limiting circuitry that limits instantaneous peak current and only shuts off the slot if the current remains out of spec for an extended time.

ORDERING INFORMATION

T_A	PACKAGE(1)
	HTSSOP (DDP)
−40°C to +85°C	TPS2343DDP

(1) Add suffix R to device type (e.g. TPS2343DDPR) to specify taped and reeled.

SIMPLIFIED BLOCK DIAGRAM



In this drawing, circuits related to many functions are oversimplified. See the Application Section of the data sheet for a more detailed representations of these functions.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)†‡

PARAMETER	TPS2343	UNIT
Input voltage range, P12VIN	−0.5 to 15	V
M12VIN	−15.0 to 0.5	
All others	−0.5 to 7	
Output voltage range, P12VO, 5VG, 3VG, 15VIOG, 3VIOG	−0.5 to V_{P12VIN} + 0.5	
P12VG	−0.5 to 28	
M12VO	−15 to 0.5	
Output current, FAULT, OUTUV, PWROFF	50	mA
Output current pulse, P12VO (dc internally limited)	3	A
M12VO	0.8	
3VAUX	2	
Operating junction temperature range, T_J	−40 to 100	°C
Storage temperature range, T_{stg}	−65 to 150	
Lead temperature soldering 1.6 mm (1/16 inch) from case for 10 seconds	260	

† Stresses beyond those listed under ”absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under ”recommended operating conditions” is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability

‡ All voltages are with respect to DIGGND.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

TEST METHOD	MIN	UNIT
Human body model (HBM)	2	kV
Charged device model (CDM)	1	kV

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	TYP	MAX	UNIT
Input supply,	M12VINA, M12VINB	−10.8	−12	−13.2	V
	P12VINA, P12VINB	10.8	12	13.2	
	DIGVCC, 3VAUXI	3.0	3.3	3.6	
	V5IN	4.75	5.00	5.25	
Load current,	PWRLEDA, PWRLEDB, ATTLEDA, ATTLEDB	0		24	mA
	P12VOA, P12VOB	0		1100	
	M12VOA, M12VOB	0		−100	
	3VAUXA, 3VAUXB	0		375	

THERMAL SHUTDOWN

PARAMETER	TYP	UNIT
Junction temperature shutdown	150	°C
Junction temperature − cooldown restart	140	°C

DISSIPATION RATING TABLE

PACKAGE	T_A	THERMAL RESISTANCE JUNCTION TO CASE Θ_{JC}	THERMAL RESISTANCE JUNCTION TO AMBIENT (NOTE 1) Θ_{JA}	THERMAL RESISTANCE JUNCTION TO AMBIENT (NOTE 2) Θ_{JA}
HTSSOP−80 (DDP)	−40 °C to 85 °C	1.4 °C/W	23 °C/W	32 °C/W

Note 1: Thermal resistance measured using an 8-layer PC board following the layout recommendations in TI Publication *PowerPAD Thermally Enhanced Package* Technical Brief SLMA002.
Note 2: Thermal resistance measured using an 8-layer PC board using only top PC board copper to spread the heat.

SERIAL MODE PINOUT

HTSSOP-80 DDP Package (Top View)



ELECTRICAL CHARACTERISTICS,

P12VIN = 12 V, DIGVCC = 3.3 V, M12VIN = −12 V, 3VAUXIN = 3.3 V, V5IN = 5 V, RMISET = 6.04 kΩ, all outputs unloaded, T_A = −40°C to 85°C, (unless otherwise noted) (1)(2)(3)

5-V Main Supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
5VS−5VIS overcurrent threshold (5 V)		43	53	63	mV
5VIS voltage fault threshold		4.25	4.5	4.75	V
5VS input bias current	PWREN = high	−100		100	µA
5VIS input bias current	PWREN = high	100	250	400	
5VIS bleed current	PWREN = low, 5VIS = 5V	8	60		mA
5VG charge current	PWREN = high, 5VG = 5 V	−70	−100	−130	µA
5VG discharge resistance	0.1 V < V_{5VG} < 0.5 V	1.5	4	15	Ω
5VG good threshold		11	11.5	12	V
V5IN supply current			2	6	mA
5VIS low comparator threshold	PWREN = low	0.075	0.100	0.150	V

3.3-V Main Supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
3VS−3VIS overcurrent threshold (3.3 V)		48	63	76	mV
3VIS voltage fault threshold		2.5	2.7	2.9	V
3VS input bias current	PWREN = high	−100		100	µA
3VIS input bias current	PWREN = high	100	290	400	
3VIS bleed current	PWREN = low, 3VIS = 3.3 V	8	40		mA
3VG charge current	PWREN = high, 3VG = 5 V	−70	−100	−130	µA
3VG discharge resistance	0.1 V < V_{3VG} < 0.5 V	1.5	4	15	Ω
DIGVCC supply current			1.2	3	mA
3VIS low comparator threshold	PWREN = low	0.075	0.100	0.150	V

ELECTRICAL CHARACTERISTICS,

P12VIN = 12 V, DIGVCC = 3.3 V, M12VIN = −12 V, 3VAUXIN = 3.3 V, V5IN = 5 V, RMISET = 6.04 kΩ, all outputs unloaded, T_A = −40°C to 85°C, (unless otherwise noted) (1)(2)(3)

12-V Main Supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
12-V internal switch on resistance	$T_A = T_J$ = 25°C, P12VG > 18 V		0.18	0.30	Ω
	T_A = −40 °C to 85 °C, P12VG > 18 V			0.4	
12-V overcurrent threshold		1.25	1.50	1.75	A
P12VIN supply current, outputs off	PWREN = low		1.8	3	mA
P12VG gate good threshold		17.5	19.0	20.5	V
P12VO fault threshold	After P12VG and 5V3VG good	9.75	10.15	10.45	
P12VG gate charge current	PWREN = high	−5	−10	−20	µA
P12VG gate discharge resistance	0.1 V < V_{P12VG} < 0.5V	1.5	4	15	Ω
Turn-on time	PWREN = high to P12VO = 11.4 V, C_{P12VG} = 22 nF		28	55	ms
	PWREN = high to P12VO = 11.4 V, C_{P12VG} = 0 nF		0.5	2.0	
Turn-off time	PWREN = low to P12VO low comparator trip, C_{P12VG} = 22 nF		1.5	3.5	µs
P12VO bleed current	PWREN = low, P12VO = 12 V	8	20		mA
P12VO low comparator threshold	PWREN = low	0.075	0.100	0.150	V
P12VO turn-on slew rate	C_{P12VG} = 0 pF, 10% to 90% measurement	2			V/ms

−12-V Main Supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
−12-V internal switch on-resistance	$T_A = T_J$ = 25°C, steady state		0.50	0.75	Ω
	T_A = −40 °C to 85 °C, steady state			0.9	
−12-V overcurrent threshold		0.15	0.20	0.25	A
M12VIN supply current, outputs off	PWREN = low		1000	2000	µA
M12VO turn-on slew rate(4)	C_{P12VG} = 22 nF, 10% to 90% measurement	0.30	0.68	1.10	V/ms
Turn-on time	C_{P12VG} = 22 nF, PWREN = high to M12VO = −10.4 V, R_L = 120 Ω	12	18	37	ms
Turn-off time	PWREN = low to M12VO low comparator trip		1.5	3.5	µs
M12VO bleed current	PWREN = low, M12VO = −12 V	−8	−20		mA
M12VO low comparator threshold	PWREN = low	−0.075	−0.100	−0.150	V

NOTES: (1). All voltages are with respect to DIGGND unless otherwise stated.
(2) Currents are positive into and negative out of the specified terminal.
(3) When references to lines of individual slots are given without the slot identifier, the statement applies to lines on each slot.
(4) −12-V main supply turn on is controlled by the +12-V main supply turn on, so the –12-V main supply slew rate is a function of C_{P12VG}.

ELECTRICAL CHARACTERISTICS,

P12VIN = 12 V, DIGVCC = 3.3 V, M12VIN = −12 V, 3VAUXIN = 3.3 V, V5IN = 5 V, RMISET = 6.04 kΩ, all outputs unloaded, T_A = −40°C to 85°C, (unless otherwise noted) (1)(2)(3)

V_{IO} Supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
15VG, 3VIOG output voltage high		11.5	11.9		V
VIOS – VIOIS overcurrent threshold (1.5 V operation)		20.0	23.5	27.0	mV
15VIOG, 3VIOG turn-off resistance	PWREN = low, 0.1 V < V_{VIOG}, V_{VIOG} < 0.5 V	10	50	100	Ω
VIOS input bias current	PWREN = high, VIOSEL = low, test circuit Figure 7	−100	20	100	µA
VIOIS input bias current	PWREN = high, VIOSEL = low, test circuit Figure 7	−100	20	200	
VIOIS bleed current	PWREN = low, VIOIS =1.5 V	8	20		mA
VIOIS low comparator threshold	PWREN = low	0.075	0.100	0.150	V
VIOIS fault threshold		1.275	1.325	1.375	
15VIOG low voltage	PWREN = low		0.1	1.0	
15VIOG, 3VIOG gate charge current		7	10	13	µA

Power Fault Response

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overcurrent fault detection time	12 V	2		6.5	µs
	−12 V, i = 250 mA	4		12	
Overcurrent response time to regulate	5 V, 3.3 V, Vio		1	3	
Overcurrent fault detection time	5 V, 3.3 V, Vio	3		8	ms
Overcurrent fault clearing time	5 V, 3.3 V, Vio	50		150	µs

NOTES: (1) All voltages are with respect to DIGGND unless otherwise stated.
(2) Currents are positive into and negative out of the specified terminal.
(3) When references to lines of individual slots are given without the slot identifier, the statement applies to lines on each slot.

ELECTRICAL CHARACTERISTICS,

P12VIN = 12 V, DIGVCC = 3.3 V, M12VIN = −12 V, 3VAUXIN = 3.3 V, V5IN = 5 V, RMISET = 6.04 kΩ, all outputs unloaded, T_A = −40°C to 85°C, (unless otherwise noted) (1)(2)(3)

3.3 VAUX and PME

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
3VAUX overcurrent threshold		0.8	1.1	1.45	A
3VAUXI to 3VAUX switch on resistance	SW = low, 3VAUXG = 10 V		300	400	mΩ
3VAUXI undervoltage threshold	SW = low	1.9	2.2	2.9	V
3VAUXI supply current, $3V_{AUX}$ off	SW = high		1000	2000	µA
3VAUXG turn-on current	SW = low, 3VAUXG = 3.3 V	−3	−5	−7	
3VAUXG turn-off resistance	SW = high, 0.1 V < 3VAUXG < 0.5 V	3	8	30	Ω
3VAUX turn-on time with no gate capacitor	C_{3VAUXG} = 0 pF, 10% to 90% measurement		200	350	µs
3VAUX turn-on slew rate with gate capacitor	C_{3VAUXG} = 22 nF, 10% to 90% measurement	0.13	0.23	0.32	V/ms
3VAUX bleed current	SW = high, 3VAUX = 3.0 V	8	28		mA
3VAUX turn-off time from SW	From SW > 2.0 V to 3VAUX < 0.5 V, C_{3VAUXG} = 22 nF		1.2	5.0	ms
3VAUX turn-off time from Fault	From 3VAUX overcurrent fault		17	25	µs
PME turn-on time from 3VAUX	From 3VAUX > 3.0 V, C_{3VAUX} = 150 µF	6	10	17	ms
PME turn-off time from SW	From SW > 2.0 V			4	µs
PME turn-off time from Fault	From 3VAUX overcurrent fault			4	
PME switch on resistance	SW = low		10	20	Ω
3VAUX output rising threshold to PME switch closed		2.5		3.0	V

DC Logic Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input high voltage (all digital inputs)		2.0			V
Input low voltage (all digital inputs)				0.8	
Input hysteresis (PGOOD)		0.15		0.60	
Output high voltage (all push-pull outputs)	I_L = 4 mA	2.4	2.8		
Output low voltage ($\overline{ATTLED}$, $\overline{PWRLED}$)	I_L = 8 mA			0.5	
	I_L = 24 mA		0.4	0.8	
Output low voltage (all other outputs)	I_L = 4 mA		0.2	0.5	
Input pull-up resistor impedance	For inputs with pull-up resistors (see pin descriptions)	30		200	kΩ
PCIXCAP threshold between 33 MHz and 533 MHz		0.3	0.4	0.5	V
PCIXCAP threshold between 533 MHz and 266 MHz		1.1	1.2	1.3	
PCIXCAP threshold between 266 MHz and 66 MHz		1.95	2.05	2.15	
PCIXCAP threshold between 66 MHz and 133 MHz		2.8	2.9	3.0	

NOTES: (1). All voltages are with respect to DIGGND unless otherwise stated.
(2) Currents are positive into and negative out of the specified terminal.
(3) When references to lines of individual slots are given without the slot identifier, the statement applies to lines on each slot.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	3VAUXGA	I/O	This pin is connected to the gate of the slot A 3VAUX internal power FET. Connect a capacitor from this pin to PWRGND to program the slot A 3VAUX ramp rate. The recommended capacitor value is 22 nF for 0.23 V/ms ramp rate.
2	3VAUXA	O	This output supplies 3VAUX power to slot A when enabled and is pulled low by an internal FET when there is a fault on slot A 3VAUX or when SWA is opened.
3	3VAUXI	I	Connect this power input to 3.3 V power to drive 3VAUX loads. Connect a 0.1-µF capacitor from this pin to PWRGND.
4	3VAUXGB	I/O	This pin is connected to the gate of the slot B 3VAUX internal power FET. Connect a capacitor from this pin to PWRGND to program the slot B 3VAUX ramp rate. The recommended capacitor value is 22 nF for 0.23 V/ms ramp rate.
5	3VAUXB	O	This output supplies 3VAUX power to slot B when enabled and is pulled low by an internal FET when there is a fault on slot B 3VAUX or when SWB is opened.
6	3VGB	I/O	Gate drive for the 3-V slot B FET switch. Ramp rate is programmed by an external capacitor in series with a 15-kΩ resistor connected from this pin to PWRGND. A capacitor value of 270 nF sets 0.37 V/ms ramp rate.
7	3VISB	I	This pin in conjunction with the 3VSB pin senses the current to the 3.3-V slot B. It connects to the load side of the 3.3-V current sense resistor. The recommended current sense resistor value is 6 mΩ. When PWRENB is false or $\overline{\text{FAULTB}}$ is true, this pin is discharged to PWRGND by an internal FET. A 0.01-µF capacitor from this pin to ANAGND is recommended.
8	3VSB	I	This pin in conjunction with the 3VISB pin senses the current to the 3.3-V slot B main power load. Connect to the source of the 3.3-V FET switch. A 0.01-µF capacitor from this pin to ANAGND is recommended.
9	3VIOGB	I/O	Gate drive for the 3.3-V V_{IO} slot B FET switches. Ramp rate is programmed by the external capacitor connected from 3VIOGB to PWRGND. The recommended capacitor value is 22 nF for a 0.45 V/ms ramp rate.
10	PWRGND1	GND	Ground for high-current paths including discharge current of external gate capacitors.
11	15VIOGB	I/O	Gate drive for the 1.5-V V_{IO} slot B FET switches. Ramp rate is programmed by the external capacitor connected from 15VIOGB to PWRGND. The recommended capacitor value is 22 nF for a 0.45 V/ms ramp rate.
12	VIOISB	I	This pin in conjunction with the VIOSB pin senses the current to V_{IO} slot B. It connects to the load side of the V_{IO} current sense resistor. The recommended current sense resistor value is 6 mΩ. When PWRENB is false or $\overline{\text{FAULTB}}$ is true, this pin is discharged to PWRGND by an internal FET. A 0.01-µF capacitor from this pin to ANAGND is recommended.
13	VIOSB	I	This pin in conjunction with the VIOISB pin senses the current to V_{IO} slot B. Connect to the current sense resistor at the Vio FET switch. A 0.01-µF capacitor from this pin to ANAGND is recommended.
14	5VISB	I	This pin in conjunction with the 5VSB pin senses the current to the 5-V slot B main power load. It connects to the load side of the 5-V current sense resistor. The recommended current sense resistor value is 6 mΩ. When PWRENB is false or $\overline{\text{FAULTB}}$ is true, this pin is discharged to PWRGND by an internal FET. A 0.01-µF capacitor from this pin to ANAGND is recommended.
15	5VSB	I	This pin in conjunction with the 5VISB pin senses the current to the 5-V slot B main power load. It connects to the source of the 5-V FET switch. A 0.01-µF capacitor from this pin to ANAGND is recommended.
16	5VGB	I/O	Gate drive for the 5-V slot B FET switch. Ramp rate is programmed by an external capacitor in series with a 15-kΩ resistor connected from this pin to PWRGND. A capacitor value of 270 nF sets 0.37 V/ms ramp rate.
17	P12VINB	I	The 12-V power input to slot B. This input must be connected to P12VINA. Connect a 0.1-µF capacitor from this pin to PWRGND.
18	P12VGB	I/O	This pin is connected to the gate of the slot B 12-V internal power FET. Connect a capacitor from this pin to PWRGND to program the slot B 12-V and −12-V power ramp rate. The recommended capacitor value is 22 nF for 0.45 V/ms ramp rate on 12 V and a 0.68 V/ms ramp rate on −12-V power.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
19	P12VOB	O	This output delivers 12-V power to slot B when enabled and is pulled to PWRGND by an internal FET when PWRRNB is false or FAULTB is true.
20	M12VINB	I	Connect this power input to −12-V power to drive slot B. This input must be connected to M12VINA. Connect a 0.1-µF capacitor from this pin to PWRGND.
21	M12VOB	O	This output delivers −12-V power to slot B when enabled and is pulled to PWRGND by an internal FET when PWRRNB is false or FAULTB is true. Turn-on of −12-V power tracks turn-on of 12-V power and is controlled by the capacitor on P12VGB.
22	MISET	I/O	This pin programs current limit for 12-V, 5-V, 3.3-V, and −12-V main supplies. MISET does not control 3.3VAUX or V_{IO} current limit. The recommended resistor from MISET to ANAGND is 6.04 kΩ ±1%. Increasing the value of this resistor raises the current-limit thresholds for the supplies listed above proportionately. MISET resistor is 12 kΩ maximum.
23	ANAGND1	GND	Ground for low-level signals including the current sense circuits and the voltage reference.
24	PCIXCAP1B	O	This pin indicates bit 1 of the PCIXCAPB state.
25	DIGGND2	GND	This pin is the ground return for the digital circuits in the TPS2343.
26	PCIXCAP2B	O	This pin indicates bit 2 of the PCIXCAPB state.
27	$\overline{\text{FAULTB}}$	O	This is an open-drain output that is low if there is a fault on the main power to slot B. This pin has an internal 100-kΩ pull-up resistor to DIGVCC.
28	$\overline{\text{AUXFLTB}}$	O	This open-drain output is low if there is a fault on V_{AUX} power to slot B. This pin has an internal 100-kΩ pull-up resistor to DIGVCC and hysteresis.
29	$\overline{\text{OUTUVB}}$	O	This open-drain output is low if slot B outputs are below normal operating range. This pin has an internal 100-kΩ pull-up resistor to DIGVCC.
30	PCIXCAP3B	O	This pin indicates bit 3 of the PCIXCAPB state.
31	PCIXCAPB	I	This pin is the input to a 5-level A/D converter that determines the speed and mode of the inserted B slot card based on the impedance from this pin to ANAGND. The operation of this pin meets the specifications of the PCI−X Local Bus Specification, revision 2.0.
32	$\overline{\text{PWROFFB}}$	O	This output is low when all of the slot B power outputs are discharged.
33	PWRENB	I	This pin enables main power for slot B when high. This pin has an internal 100-kΩ pull-up resistor to DIGVCC and hysteresis. When low, FAULTB is clearded and OUTUVB is asserted.
34	SWB	I	This input enables 3.3-V V_{AUX} power to slot B. When low, $\overline{\text{AUXFLTB}}$ is cleared. This pin has an internal 100-kΩ pull-up resistor to 3VAUXI and hysteresis.
35	$\overline{\text{ATTLEDB}}$	O	This output is an open-drain power output that directly drives the slot B attention indicator LED. This pin indicates the slot B LED attention indicator output signal from ALEDENB. This signal pulls low with up to 24 mA of drive when asserted and is pulled high by an on-chip 100-kΩ resistor to V5IN when deasserted.
36	$\overline{\text{PWRLEDB}}$	O	This open-drain active-low power output directly drives the slot B power indicator LED. This pin indicates the slot B power LED output from PLEDENB. This signal pulls low with up to 24 mA of drive when asserted and is pulled high by an on-chip 100-kΩ resistor to V5IN when deasserted.
37	VIOSELB	I	This pin selects 3.3 V V_{IO} for slot B when high, 1.5 V when low.
38	ALEDENB	I	This pin controls ATTLEDB. When this input is high, the LED is on (low).
39	PLEDENB	I	This pin controls PWRLEDB. When this input is high, the LED is on (low).
40	DIGVCC	I	This pin is the 3.3-V main power input to the TPS2343. Bypass this pin to DIGGND with a 0.1-µF ceramic capacitor close to the TPS2343.
41	DIGGND1	GND	This pin is the ground return for the digital circuits in the TPS2343.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
42	PLEDENA	I	This pin controls PWRLEDA. When this input is high, the LED is on (low).
43	ALEDENA	I	This pin controls ATTLEDA. When this input is high, the LED is on (low).
44	VIOSELA	I	This pin selects 3.3 V V_{IO} for slot A when high, 1.5 V when low.
45	$\overline{\text{PWRLEDA}}$	O	This output is an open−drain active−low power output that directly drives the slot A power indicator LED. This pin indicates the slot A power LED output from PLEDENA. This signal pulls low with up to 24 mA of drive when asserted and is pulled high by an on-chip 100-kΩ resistor to V5IN when deasserted.
46	$\overline{\text{ATTLEDA}}$	O	This open-drain power output directly drives the slot A attention indicator LED. This pin indicates the slot A LED attention indicator output signal from ALEDENA. This signal pulls low with up to 24 mA of drive when asserted and is pulled high by an on-chip 100-kΩ resistor to V5IN when deasserted.
47	SWA	I	This input enables 3.3-V Aux power to slot A. When low, $\overline{\text{AUXFLTA}}$ is cleared. This pin has an internal 100-kΩ pull-up resistor to 3VAUXI and hysteresis.
48	PWRENA	I	This pin enables main power for slot A when high. When low, $\overline{\text{FAULTA}}$ is cleared and $\overline{\text{OUTUVA}}$ is asserted. This pin has an internal 100-kΩ pull-up resistor to DIGVCC and hysteresis.
49	$\overline{\text{PWROFFA}}$	O	This output is low when all of the slot A power outputs are discharged.
50	PCIXCAPA	I	This pin is the input to a 5-level A/D converter that determines the speed and mode of the inserted A slot card based on the impedance from this pin to ANAGND. The operation of this pin meets the specifications of the PCI−X Local Bus Specification, revision 2.0.
51	PCIXCAP3A	O	This pin indicates bit 3 of the PCIXCAPA state.
52	$\overline{\text{OUTUVA}}$	O	This open−drain output is low if slot A main outputs are below normal operating range. This pin has an internal 100-kΩ pull-up resistor to DIGVCC.
53	$\overline{\text{AUXFLTA}}$	O	This is an open-drain output that is low if there is a fault on V_{AUX} power to slot A. This pin has an internal 100-kΩ pull-up resistor to DIGVCC.
54	$\overline{\text{FAULTA}}$	O	This is an open-drain output that is low if there is a fault on the main power to slot A. This pin has an internal 100-kΩ pull-up resistor to DIGVCC.
55	PCIXCAP2A	O	This pin indicates bit 2 of the PCIXCAPA state.
56	DIGGND3	GND	This pin is the ground return for the digital circuits in the TPS2343.
57	PCIXCAP1A	O	This pin indicates bit 1 of the PCIXCAPA state.
58	PGOOD	I	This input is asserted when power is good in the whole system. This pin has an internal 100-kΩ pull-up resistor to DIGVCC and hysteresis.
59	ANAGND2	GND	Ground for low-level signals including the current sense circuits and the voltage reference.
60	M12VOA	O	This output delivers −12-V power to slot A when enabled and is pulled to PWRGND by an internal FET when PWRENA is false or $\overline{\text{FAULTA}}$ is true. Turn-on of −12-V power tracks turn-on of 12-V power and is controlled by the capacitor on P12VGA.
61	M12VINA	I	Connect this power input to −12-V power to drive slot A. This input must be connected to M12VINB. Connect a 0.1-µF capacitor from this pin to PWRGND.
62	P12VOA	O	This output delivers 12-V power to slot A when enabled and is pulled to PWRGND by an internal FET when PWRENA is false or $\overline{\text{FAULTA}}$ is true.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
63	P12VGA	I/O	This pin is connected to the gate of the slot A 12-V internal power FET. Connect a capacitor from this pin to PWRGND to program the slot A 12-V and −12-V power ramp rate. The recommended capacitor value is 22 nF for 0.45-V/ms ramp rate on 12 V and a 0.68-V/ms ramp rate on −12-V power.
64	P12VINA	I	The 12-V power input to slot A. This input must be connected to P12VINB. Connect a 0.1-µF capacitor from this pin to PWRGND.
65	5VGA	I/O	Gate drive for the 5-V slot A FET switch. Ramp rate is programmed by an external capacitor in series with a 15-Ω resistor connected from this pin to PWRGND. A capacitor value of 270 nF sets 0.37-V/ms ramp rate.
66	5VSA	I	This pin in conjunction with the 5VISA pin senses the current to the 5-V slot A. It connects to the source of the 5-V FET switch. A 0.01-µF capacitor from this pin to ANAGND is recommended.
67	5VISA	I	This pin in conjunction with the 5VSA pin senses the current to the 5-V slot A. It connects to the load side of the 5-V current sense resistor. The recommended current sense resistor value is 6mΩ. When PWRENA is false or $\overline{\text{FAULTA}}$ is true, this pin is discharged to PWRGND by an internal FET. A 0.01-µF capacitor from this pin to ANAGND is recommended.
68	VIOSA	I	This pin in conjunction with the VIOISA pin senses the current to V_{IO} slot A. Connect to the current sense resistor at the Vio FET switch. A 0.01-µF capacitor from this pin to ANAGND is recommended.
69	VIOISA	I	This pin in conjunction with the VIOSA pin senses the current to V_{IO} slot A. It connects to the load side of the V_{IO} current sense resistor. The recommended current sense resistor value is 6 mΩ. V_{IO} bleed is connected to this pin. A 0.01-µF capacitor from this pin to ANAGND is recommended.
70	15VIOGA	I/O	Gate drive for the 1.5-V V_{IO} slot A FET switches. Ramp rate is programmed by the external capacitor connected from 15VIOGA to PWRGND. The recommended capacitor value is 22 nF for a 0.45-V/ms ramp rate.
71	PWRGND2	GND	Ground for high-current paths including discharge current of external gate capacitors.
72	V5IN	I	Connect this power input to 5-V power. This input is used to bias analog circuits. Connect a 0.1-µF capacitor from this pin to PWRGND.
73	3VIOGA	I/O	Gate drive for the 3.3-V V_{IO} slot A FET switches. Ramp rate is programmed by the external capacitor connected from 3VIOGA to PWRGND. The recommended capacitor value is 22 nF for a 0.45-V/ms ramp rate.
74	3VSA	I	This pin in conjunction with the 3VISA pin senses the current to the 3.3-V slot A main power load. Connect to the source of the 3.3-V FET switch. A 0.01-µF capacitor from this pin to ANAGND is recommended.
75	3VISA	I	This pin in conjunction with the 3VSA pin senses the current to the 3.3-V slot A. It connects to the load side of the 3.3-V current sense resistor. The recommended current sense resistor value is 6 mΩ. When PWRENA is false or $\overline{\text{FAULTA}}$ is true, this pin is discharged to PWRGND by an internal FET. A 0.01-µF capacitor from this pin to ANAGND is recommended.
76	3VGA	I/O	Gate drive for the 3.3-V slot A FET switch. Ramp rate is programmed by an external capacitor in series with a 15-kΩ resistor connected from this pin to PWRGND. A capacitor value of 270 nF sets 0.37-V/ms ramp rate.
77	$\overline{\text{PMEA}}$	I	This input connects to the slot A power management event (PME) signal. This pin is internally pulled up to 3VAUXA with a 100-kΩ resistor.
78	$\overline{\text{PMEOA}}$	O	This output is connected to $\overline{\text{PMEA}}$ by a bus switch that is closed after slot A 3VAUX voltage is good and opens immediately when there is a fault on slot A 3VAUX or SWA opens.
79	$\overline{\text{PMEOB}}$	O	This output is connected to $\overline{\text{PMEB}}$ by a bus switch that is closed after slot B 3VAUX voltage is good and opens immediately when there is a fault on slot B 3VAUX or SWB opens.
80	$\overline{\text{PMEB}}$	I	This input connects to the slot B power management event (PME) signal. This pin is internally pulled up to 3VAUXB with a 100-kΩ resistor.

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Turn-On Sequence

Main power to the slot turns on when all input supplies are active and power is commanded, by asserting PWRENx. The charge pump combined with the P12VGx capacitor produces a linear voltage ramp on P12VGx, which produces a linear ramping of the 12-V output and the −12-V output. At the same time, a current source on 5VG combined with the 5VG capacitor produces a linear voltage ramp on 5VG and a current source on 3VG combined with the 3VG capacitor produces a linear voltage ramp on 3VG, which produces a linear ramping of the 3.3-V and 5-V main outputs.

During this time, if any main slot current exceeds the appropriate over-current threshold for more than the over-current sensitivity time, the slot latches off and remains off until the logic command is turned off and on again.

When P12VGx exceeds the 12-V gate good threshold, 5VG exceeds the 5-V good threshold, and 3VG exceeds the 3-V gate good threshold, outputs should be fully ramped and the power MOSFETs should be fully enhanced.

+12-V Supply Control

The TPS2343 integrates an N-channel power MOSFET for the 12-V supply and a voltage multiplying charge pump to drive the gate of the power MOSFET to 20 V. Inrush current for the 12-V supply is controlled because the slew rate of the 12-V supply is limited. The slew rate for the 12-V supply is set by the capacitor from P12VG to AGND.

Slew rate can be estimated as:

$$\frac{dV}{dt} = \frac{I_{GATE}}{C_{P12VGx}}$$

where C_{P12VGx} is the capacitor from P12VGx to AGND and I_{GATE} is the P12VGx gate charge current.

PCI specifications allow for 12-V supply adapter card bulk capacitance of up to 300 µF. This load capacitance causes additional inrush current of:

$$I_{INRUSH} = C_{LOAD} \times \frac{dV}{dt} = 300\ \mu F \times \frac{I_{GATE}}{C_{P12VGx}}$$

Using the recommended value for C_{P12VGx} = 0.022 µF and the typical value for I_{GATE} = 10 µA, average inrush current can be estimated as:

$$I_{INRUSH} = 300\ \mu F \times \frac{10\ \mu A}{0.022\ \mu F} = 0.136\ A$$

An internal current−sense circuit monitors the 12-V supply. The over-current threshold for the 12-V supply is directly proportional to the resistor from MISET to AGND. Raising the MISET resistor simultaneously raises the current limit threshold for the 12-V, 5-V, 3.3-V and −12-V supplies. For example, to raise the nominal output current from the 12-V supply by 20%, increase the MISET resistor 20%. This resistor can be as high as 12 kΩ if necessary.

APPLICATION INFORMATION

−12-V Supply Control

The TPS2343 integrates an N-channel power MOSFET for the −12-V supply. This switch turns on when PWRENx is asserted and turns off when PWRENx is deasserted or when there is a fault on any main power supply to the slot.

Like the 12-V supply, inrush for the −12-V supply is controlled by controlling turn-on slew rate. The −12-V supply tracks the 12-V supply, so the slew rates of these supplies are directly related. To insure that the power MOSFET for the −12-V supply fully enhances, the tracking amplifier has a gain of approximately 1.4, producing a −12-V supply slew rate 40% higher than the 12-V supply slew rate.

PCI specifications allow for −12-V supply adapter card bulk capacitance of up to 150 μF. This load capacitance causes additional inrush current of:

$$I_{INRUSH} = C_{LOAD} \times \frac{dV}{dt} = 150\ \mu F \times \frac{I_{GATE}}{C_{P12VG}} \times 1.4$$

Using the recommended value for C_{P12VG} = 0.022 μF and the typical value for I_{GATE} = 10 μA, average inrush current can be estimated as:

$$I_{INRUSH} = 150\ \mu F \times \frac{10\ \mu A}{0.022\ \mu F} \times 1.4 = 0.095\ A$$

An internal current-sense circuit monitors the −12-V supply. The over-current threshold for the −12-V supply is directly proportional to the resistor from MISET to AGND. Raising the MISET resistor simultaneously raises the current limit threshold for the 12-V, 5-V, 3.3-V and −12-V supplies. For example, to raise the nominal output current from the −12-V supply by 20%, increase the MISET resistor 20%. This resistor can be as high as 12 kΩ if necessary.

+5-V Main Supply Control

The TPS2343 uses external N-channel power MOSFETs for the 5-V supply. Inrush current for this supply is controlled because the slew rate of the supplies is limited. This slew rate is set by the capacitor from 5VGx to AGND. Slew rate can be estimated as:

$$\frac{dV}{dt} = \frac{I_{GATE}}{C_{5VG}}$$

where C_{5VG} is the capacitor from 5VGx to AGND and I_{GATE} is the 5VGx gate charge current.

PCI specifications allow for 5-V supply adapter card bulk capacitance of up to 3000 μF. This load capacitance causes additional inrush current of:

$$I_{INRUSH} = C_{LOAD} \times \frac{dV}{dt} = 3000\ \mu F \times \frac{I_{GATE}}{C_{5VGx}}$$

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Using the recommended value for C_{5VGx} = 0.27 µF and the typical value for I_{GATE} = 100 µA, average inrush current can be estimated as:

$$I_{INRUSH} = 3000\ \mu F \times \frac{100\ \mu A}{0.27\ \mu F} = 1.11\ A$$

An external current-sense resistor monitors the 5-V supply. The calculation of external resistor values is shown in the determining component values section. The over-current thresholds is directly proportional to the resistor from MISET to AGND and inversely proportional to the current-sense resistor. Raising the MISET resistor simultaneously raises the current limit threshold for the 12-V, 5-V, 3.3-V and −12-V supplies. This resistor can be as high as 12 kΩ if necessary.

+3.3-V Main Supply Control

The TPS2343 uses external N-channel power MOSFETs for the 3.3-V supply. Inrush current for this supply is controlled because the slew rate of the supply is limited. These slew rates are set by the capacitor from 3VGx to AGND. Slew rate can be estimated as:

$$\frac{dV}{dt} = \frac{I_{GATE}}{C_{3VGx}}$$

where C_{3VGx} is the capacitor from 3VGx to AGND and I_{GATE} is the 3VGx gate charge current.

PCI specifications allow for 3.3-V supply adapter card bulk capacitance of up to 3000 µF. This load capacitance causes additional inrush current of:

$$I_{INRUSH} = C_{LOAD} \times \frac{dV}{dt} = 3000\ \mu F \times \frac{I_{GATE}}{C_{3VGx}}$$

Using the recommended value for C_{3VGx} = 0.27 µF and the typical value for I_{GATE} = 100 µA, average inrush current can be estimated as:

$$I_{INRUSH} = 3000\ \mu F \times \frac{100\ \mu A}{0.27\ \mu F} = 1.11\ A$$

An external current-sense resistor monitors the 3.3-V supply. The calculation of external resistor values is shown in the determining component values section.The over-current threshold is directly proportional to the resistor from MISET to AGND and inversely proportional to the current-sense resistor. Raising the MISET resistor simultaneously raises the current limit threshold for the 12-V, 5-V, 3.3-V and −12-V supplies. This resistor can be as high as 12 kΩ if necessary.

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+1.5-V and +3.3-V V_{IO} Supply Control

V_{IO} is frequently used to power V_{IO} for both the slot and the bridge so that there is minimal drop between the slot and the bridge V_{IO} supplies. When calculating the current-limit threshold for V_{IO}, take into account the current consumption of the slot and the bridge.

The TPS2343 uses external N-channel power MOSFETs for the 1.5-V and 3.3-V V_{IO} supplies. Inrush current for these supplies is controlled because the slew rate of the supplies are limited. Refer to the VIO Power Selection in the Application Section.

Both 1.5-V and 3.3-V VIO slew rates are usually set to the same value capacitor, C_{VIOGx} to AGND and on 3_{VIOGx} to AGND. I_{GATE} is 10 μA for both 15VIOGx and 3VIOGx. Slew rate can be estimated as:

$$\frac{dV}{dt} = \frac{I_{GATE}}{C_{VIOGx}}$$

PCI specifications allow for 1.5-V and 3.3-V V_{IO} supply adapter card bulk capacitance of up to 150 μF. This load capacitance causes additional inrush current of:

$$I_{INRUSH} = C_{LOAD} \times \frac{dV}{dt} = 150\ \mu F \times \frac{I_{GATE}}{C_{VIOGx}}$$

Using the recommended value for C_{VIOGx} = 0.022 μF and the typical value for I_{GATE} = 5 μA, average inrush current can be estimated as:

$$I_{INRUSH} = 150\ \mu F \times \frac{10\ \mu A}{0.022\ \mu F} = 0.068A$$

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3VAUX Supply Control

The TPS2343 3VAUX supply is completely independent of the main supply. Supply status and faults on main supplies have no effect on 3VAUX and faults on 3VAUX have no effect on main supply operation.

The TPS2343 uses internal power MOSFETs for the 3VAUX supply and voltage multiplying charge pumps to drive the gates of the power MOSFETs to 8 V. Inrush current for the 3VAUX supply is controlled because the slew rate of the 3VAUX supply is limited. This slew rate is set by the capacitor from 3VAUXGx to AGND. Slew rate can be estimated as:

$$\frac{dV}{dt} = \frac{I_{GATE}}{C_{3VAUXGx}}$$

where $C_{3VAUXGx}$ is the capacitor from 3VAUXGx to AGND and IGATE is the 3VAUXG gate charge current. Inrush current caused by this slewing and any adapter card load capacitance can be estimated as:

PCI specifications allow for 3.3VAUX supply adapter card bulk capacitance of up to 150 µF. This load capacitance causes additional inrush current of:

$$I_{INRUSH} = C_{LOAD} \times \frac{dV}{dt} = C_{LOAD} \times \frac{5\ \mu A}{C_{3VAUXGx}}$$

Using the recommended value for $C_{3VAUXGx}$ = 0.022 µF and the typical value for I_{GATE} = 5 µA, average inrush current can be estamated as:

$$I_{RUSH} = 150\ \mu F \times \frac{5\ \mu A}{0.022\ \mu F} = 0.034\ A$$

The 3VAUXx current-sense threshold is internally set and can not be adjusted.

When main power is applied to the TPS2343, all gates are actively held low. When main power is removed, leakage current can potentially raise gate voltage, but because main power is not applied, no malfunction occurs. This is noted here as floating gates may be observed during bench testing, but ths is not an application problem.

APPLICATION INFORMATION

Layout Considerations

It is important to use good layout practices regarding device placement and etch routing of the backplane/system board to optimize the performance of the hot plug circuit. Some of the key considerations are listed here:

- Decoupling capacitors should be located close to the device.
- Any protection devices (e.g. zener clamps) should be located close to the device.
- To reduce insertion loss across the hot plug interface, use wide traces for the supply and return current paths. A power plane can be used for the supply return or PWRGND nodes.
- Additional copper placed at the land patterns of the sense resistors and pass FETs can significantly reduce the thermal impedance of these devices, reducing temperature rise in the module and improving overall reliability.
- Because typical values for current sense resistors can be very low (6 mΩ typical), board trace resistance between elements in the supply current paths becomes significant. To achieve maximum accuracy of the overload thresholds, good Kelvin connections to the resistors should be used for the current sense inputs to the device. The current sense traces should connect symmetrically to the sense resistor land pattern, in close proximity to the element leads, not upstream or downstream from the device.

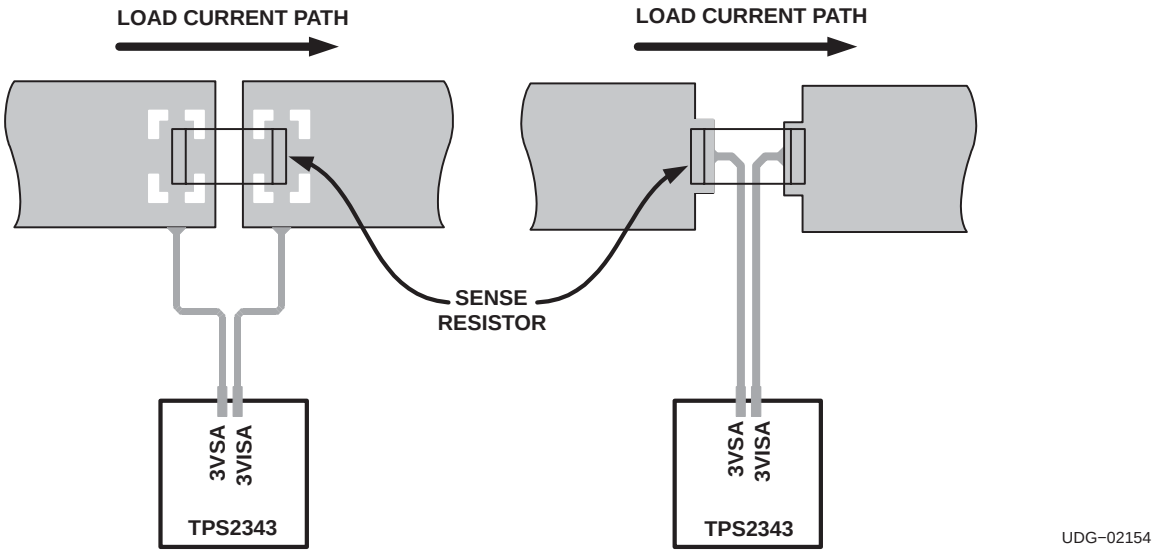


Figure 1. Connecting the Sense Resistors

These recommended layouts provide force-and-sense (Kelvin) connection to the current sense resistor to minimize circuit board trace resistance.

APPLICATION INFORMATION

Power and Grounding

Connect all TPS2343 grounds directly to the digital ground plane on the circuit board through the shortest path possible. Also connect P12VINA, P12VINB, M12VINA and M12VINB directly to the appropriate power plane through the shortest path possible. A 0.1-µF decoupling capacitor is recommended on each of these power pins, as close to the pin as possible.

Thermal Model

The TPS2343 is packaged in the HTSSOP-80 PowerPad™ small outline package. The PowerPad™ package is a thermally enhanced standard size device package designed to eliminate the use of bulky heatsinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard printed circuit board (PCB) assembly techniques, and can be removed and replaced using standard repair procedures.

The leadframe die pad is exposed on the bottom of the device. This provides an extremely low thermal resistance between the die and the thermal pad. The thermal pad can be soldered directly to the PCB for heatsinking. In addition, through the use of thermal vias, the thermal pad can be directly connected to a power plane or special heat sink structure designed into the PCB. On the TPS2343, the die substrate is internally connected to the −12-V input supply. Therefore the power plane or heatsink connected to the thermal pad on the bottom of the device must also connect to the −12-V input supply (recommended) or float independent of any supply (acceptable).

The thermal performance can be modeled by determining the thermal resistance between the die and the ambient environment. Thermal resistances are measures of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation and the lower the object's thermal resistance. Figure 3 illustrates the thermal path and resistances from the die, T_J through the printed circuit board to the ambient air.

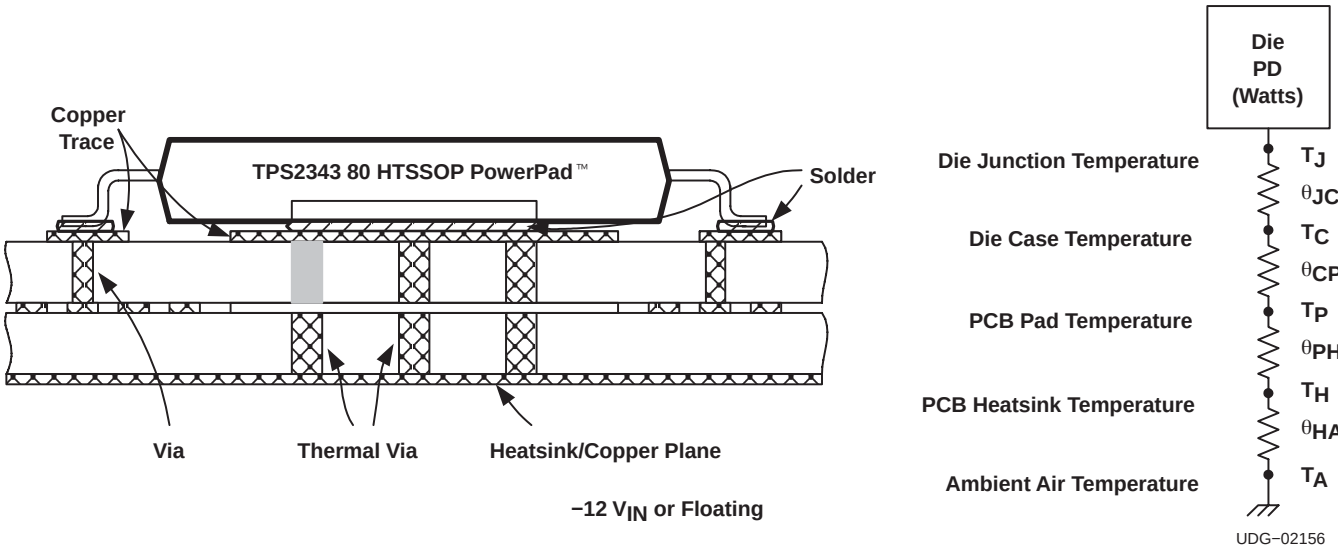
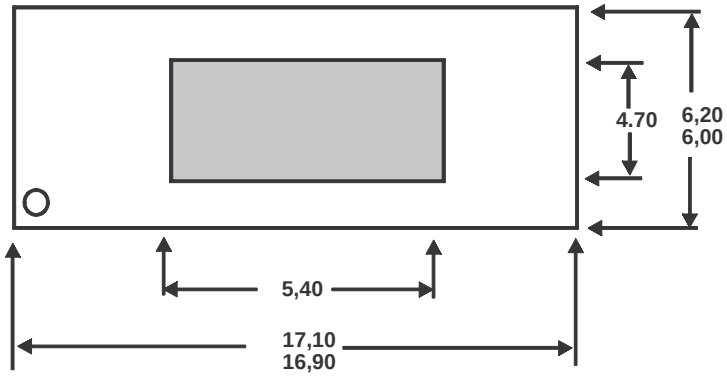


Figure 2. PowerPAD™ Thermal Model

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Technical Brief *PowerPAD™ Thermally Enhanced Package* (SLMA002) can be used as a guide to model the TPS2343 thermal resistance.

DDP PowerPad 80 Pin



NOTE:

The pad is centered in both directions with the pins. The tolerance includes both the size and the centering.

When mounted to a copper pad with solder on a PCB with two ounce traces, the TPS2343 exhibits thermal resistance from junction to ambient of 29°C/W. When the TPS2343 is mounted to a conventional PCB with solder mask under the package and only the lead tips soldered to traces, the TPS2343 exhibits thermal resistance from junction to ambient of 35°C/W.

Refer to Technical Briefs: PowerPAD™ Thermally Enhanced Package SLMA003 and PowerPAD™ Made Easy SLMA004 for more information on using this PowerPad™ package.

APPLICATION INFORMATION

Determining Component Values

Load Conditions

Table 1. Load Conditions for Determining Component Values

SUPPLY DRIVER	I_{LOAD} (A)	I_{TRIP} (A)	C_{LOAD} (µF)	SR (V/s)
+12 V	0.500	1.50	300	250
+5 V	5.000	7.00	3000	200
+3.3 V	7.600	10.0	3000	200
−12 V	0.100	0.20	150	200
+3.3 Vaux	0.375	1.10	150	5000
+1.5 VIO	1.500	4.00	150	200

+3.3-V Supply

Overload Trip Point with MISET = 6.04 kΩ

Desired I_{TRIP} (nom) ≅ 10 A

$$R_{SENSE} = \frac{V_{RTRIP\ (nom)}}{I_{TRIP\ (nom)}} = \frac{63\ mV}{10\ A} = 0.0063\ \Omega \quad \therefore \text{Choose 6 m}\Omega,\ 2\%\ \text{sense resistor}$$

$$I_{TRIP(min)} = \frac{V_{TRIP\ (min)}}{R_{SENSE\ (max)}} = \frac{48\ mV}{6.12\ m\Omega} = 7.84\ A$$

$$I_{TRIP(max)} = \frac{V_{TRIP\ (max)}}{R_{SENSE\ (min)}} = \frac{76\ mV}{5.88\ m\Omega} = 12.93\ A$$

+5-V Supply

Overload Trip Point with MISET = 6.04 kΩ

Desired I_{TRIP} (nom) ≅ 7 A

$$R_{SENSE} = \frac{V_{RTRIP\ (nom)}}{I_{TRIP\ (nom)}} = \frac{53\ mV}{7\ A} = 0.00589\ \Omega \quad \therefore \text{Choose 6 m}\Omega,\ 2\%\ \text{sense resistor.}$$

$$I_{TRIP(min)} = \frac{V_{TRIP\ (min)}}{R_{SENSE\ (max)}} = \frac{43\ mV}{6.12\ m\Omega} = 7.03\ A$$

$$I_{TRIP(max)} = \frac{V_{TRIP\ (max)}}{R_{SENSE\ (min)}} = \frac{63\ mV}{5.88\ m\Omega} = 10.71\ A$$

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3.3 Volt or 1.55 Volt Supply for V_{IO}

Overload trip point with MISET = 6.04 kΩ.

Desired $I_{TRIP(nom)}$ = 4 A

$$R_{SENSE} = \frac{V_{TRIP(nom)}}{I_{TRIP(nom)}} = \frac{23.5\ mV}{4.0\ A} = 0.00598\Omega$$

Choose 0.006 Ω

$$I_{TRIP(min)} = \frac{20\ mV}{0.00612\ \Omega} = 3.27\ A_{MIN}$$

$$I_{TRIP(max)} = \frac{27\ mV}{0.00588\ \Omega} = 4.594\ A_{MIN}$$

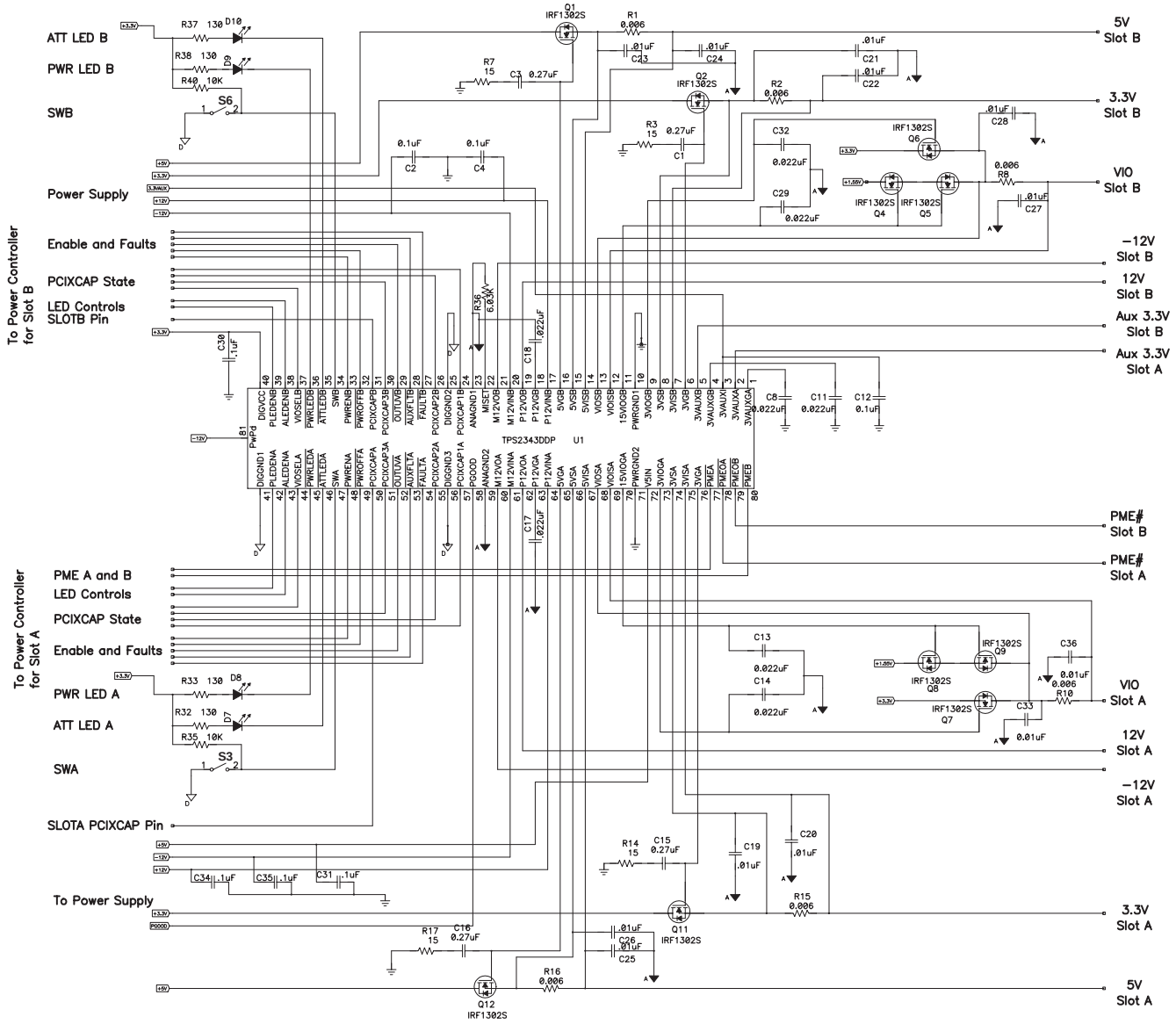
Thermal Shutdown

Under normal operating consitions, the power dissipation in the TS2343 is low enough that the junction temperature (T_J) is not more than 15°C above air temperature (T_A). However, in the case of a load that exceeds PCI specifications (but remains under the TPS2343 overcurrent threshold) power dissipation can be higher. To prevent any damage from an out-of-specification load or severe rise in ambient temperature, the TPS2343 contains two independent thermal shutdown circuits, one for each main supply slot. VAUX is not affected by the thermal shutdown.

The highest power dissipation in the TPS2343 is from the 12-V power FET so that TPS2343 temperature sense elements are integrated closely with these FETs. These sensors indicate when the temperature at these transistors exceeds approximately 150°C, due either to average device power dissipation, 12-V power FET power dissipation, or a combination of both.

When excessive junction temperature is detected in one slot, that slot's fault latch is set and remains set until the junction temperature drops by approximately 10°C and the slot is then restarted. The other slot is not affected by this event.

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MOSFET Selection

All external power MOSFETs are N-channel devices. Gate resistors are not required.

Hot plug can cause excessive voltage spikes on the input and output of the FET. During a short circuit, an excessive current spike can occur before current limit turns off the output. Although the duration is usually very small, the energy can be large and cause big voltage fluctuations. The MOSFET will operate at high current and high drain to source voltage which could violate the safe operating area of the device and cause breakdown.

To ensure safe operation of the external MOSFET, the drain-to-source voltage rating should be reasonably higher than V_{IN}. A 2-to-1 or 3-to-1 ratio of the V_{DSS} to V_{IN} is recommended.

V_{DSS} > 2 x V_{IN}

The current rating of the FET at the maximum case temperature (usually 70°C − 100°C), I_D, should be at least 2 x $I_{TRIP(max)}$ (see R_{SENSE} Calculations Section).

I_D at $T_{C(max)}$ > 2 x $I_{TRIP(max)}$

The gate-to-source voltage rating, VGS of the FET should be at least 10 V because the TPS2343 gate voltages can be as high as 12 V and the source voltage as low as 3.3 V, a difference of 8.7 V.

VGS > 10 V

Another important parameter in choosing a FET is the on-resistance, $R_{DS(on)}$. The lower the $R_{DS(on)}$, the smaller the power dissipation of the FET and the easier to maintain the PCI recommended bus voltage. The lowest $R_{DS(on)}$ FETs are the most expensive. To calculate the FET $R_{DS(on)}$, note the lower limit for each slot voltage specified in the PCI−X Electrical and Mechanical Addendum.

Table 2.

SUPPLY VOLTAGE	PCI TOLERANCE	SUPPLY TOLERANCE	MAXIMUM OPERATING CURRENT
+5 V	±0.25 V	±3%	5.0 A
+3.3 V	±0.3 V	±3%	7.6 A
VIO = 3.3	±0.3 V	±3%	3.5 A
VIO = 1.5	±0.075 V	±3%	1.5 A

APPLICATION INFORMATION

The difference between the lower limit of both the system power supply and the PCI specification slot voltage value is the system voltage budget. System power supplies specified with slightly high output voltage increases the system voltage budget making the FETs $R_{DS(on)}$ less critical. To calculate the $R_{DS(on)}$, sum the voltage drop due to contact resistance of the power input connector, the PCI connector, and the sense resistor. This sum is subtracted from the system voltage budget to give the $VR_{DS(on)}$ and ultimately the $R_{DS(on)}$.

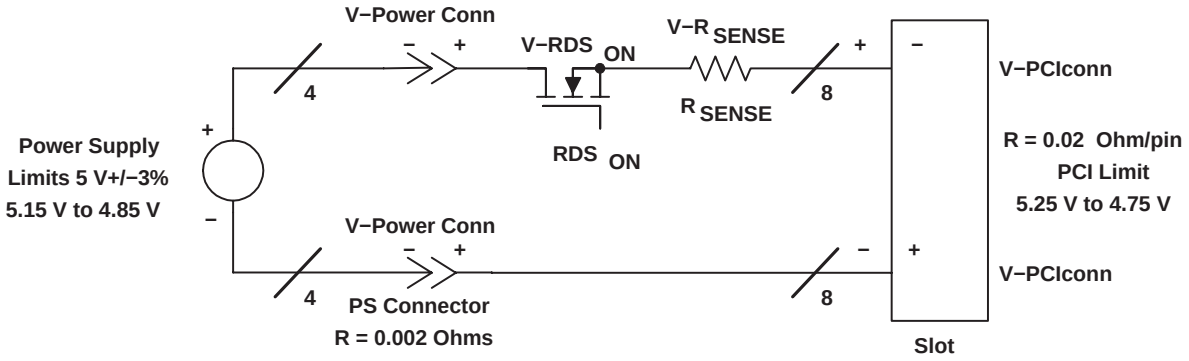


Figure 3.

Terms

Terms are defined below referenced by an example calculation.

- System voltage budget = PCI lower limit − power supply lower limit
- System voltage drop= V power connector + V PCI connector + VR_{SENSE}

(For power and ground paths)

- $VR_{DS(on)}$ = system voltage budget − system voltage drop
- $R_{DS(on)}$ = $VR_{DS(on)}$/max operating current

APPLICATION INFORMATION

Example Calculation of $R_{DS(on)}$ for the 5.0 V Main:

- PS low voltage 5.0 V − 3% = 4.85 V
- PCI spec lowest voltage to add in card = 4.75 V
- System voltage budget = 4.85 V − 4.75 V = 0.1 V
- PCI bus has 8 pins for 5.0 A, 5.0 A/8 pins = 0.625 A/pin
- Contact resistance = 20 mΩ, .625 A x 0.020 Ω = 12.5 mV
- V_{PCI} connector = 12.5 mV + 12.5 mV (return path) = 25 mV
- V power connector = 5.0 A/4 pins = 1.25 A/pin
- Pin contact resistance = 0.002 Ω,
- V power connector = 1.25A x 0.002 Ω = 2.5 mV, 2.5 mV x 2 = 5 mV
- V_{RSENSE} = 5.0 A x 0.006 Ω = 30 mV
- System voltage budget = V_{PCI} connector + V power connector + V_{RSENSE} +$VR_{DS(on)}$
- 100 = 25 + 5 + 30 + $VR_{DS(on)}$,
- $VR_{DS(on)}$ = 40 mV
- $R_{DS(on)}$ = 0.040 V/5 A = 8 mΩ

Systems have different parameters but calculating $R_{DS(on)}$ for the different voltages using these assumptions gives the following results.

Table 3.

VOLTAGE	$R_{DS(on)}$
+5 V	8 mΩ
+3.3 V	12 mΩ
+3.3 VIO	12 mΩ
+1.5 VIO	4 mΩ

FET Heatsink

Place a layer of copper on the circuit board under the surface mount FET and solder the FET to the board for good thermal connection. Connect the copper to an inner voltage layer at the same potential or if possible, an area of copper on the other side of the board.

Decoupling Capacitors

Decoupling is required on the power inputs to the TPS2343. Use 0.1-µF capacitors on the 12 V, −12 V, 5 V, 3.3 V main and 3.3-V_{AUX} and 1.5-V_{AUX} inputs and keep them close to the TPS2343 voltage input pins.

The pin descriptions for the TPS2343 signal outputs recommend 0.01-µF decoupling capacitors. These are not required.

APPLICATION INFORMATION

PCI−X Capability Selection

The PCI−X Local Bus 2.0 specification describes how the PCIXCAP pins program board operating mode using resistors on the board. The TPS2343 decodes the resistor values and communicates this to the slot controller using logic signals.

Five different operating modes are allowed under PCI−X 2.0. These modes are compatible with the three existing PCI and PCI−X 1.0 modes and add operation at 266 MHz and 533 MHz. The PCI−X 2.0 specification requires that PCIXCAP pins are pulled up to 3.3 V with a 3.3-kΩ, 5% resistor on the backplane or systemboard. This pull-up resistor combined with the resistor on the board creates a voltage divider as shown in Table 4.

Table 4.

MODE	BUS SPEED	BOARD CONNECTION ON PCIXCAP PIN	PCIXCAP PIN NOMINAL VOLTAGE
PCI 2.2	33 MHz/66 MHz	ground	0 V
PCI−X 1.0	66 MHz	10 kΩ 1% to ground	2.481 V
PCI−X 1.0	133 MHz	open circuit	3.300 V
PCI−X 2.0	266 MHz	3.16 kΩ 1% to ground	1.614 V
PCI−X 2.0	533 MHz	1.02 kΩ 1% to ground	0.779 V

The TPS2343 detects these five different modes using four comparators. These comparators have voltage thresholds between the nominal voltage points, as shown in the electrical characteristics table. These thresholds are proportional to DIGVCC voltage, so any supply variations are compensated by equivalent variation in the voltage thresholds. The voltage thresholds are far from the nominal voltage, so there is noise margin in mode selection. The table below shows these margins with a 3.3-kΩ, 5% pull-up resistor and the voltage threshold ranges shown in the electrical characteristic table.

Table 5.

MODE WINDOW	PCIXCAP VOLTAGE NOISE MARGIN
33 MHz to 533 MHz	0.279 V
533 MHz to 266 MHz	0.314 V
266 MHz to 66 MHz	0.331 V
66 MHz to 133 MHz	0.319 V

PCIXCAP Outputs

The PCIXCAPxn outputs directly communicate the PCIXCAP resistances according to Table 6.

Table 6.

MODE	BUS SPEED	PCIXCAPx1 (PINS 48, 13)	PCIXCAPx2 (PINS 46, 15)	PCIXCAPx3 (PINS 43, 18)
PCI 2.2	33 MHz/66 MHz	0	0	0
PCI−X 1.0	66 MHz	1	0	0
PCI−X 1.0	133 MHz	1	1	0
PCI−X 2.0	266 MHz	0	0	1
PCI−X 2.0	533 MHz	1	0	1

If desired, PCIXCAPx3 can be connected to VIOSEL through an inverter to automatically set VIO based on adapter card type.

APPLICATION INFORMATION

Power Stage Design

Adapter card current is a combination of static adapter card current consumption plus inrush current caused by the supply voltage ramping into the adapter card decoupling capacitance. The TPS2343 implements current limiting on each supply. For the 5-V, 3.3-V and VIO supplies, user-supplied 6-mΩ resistors sense current. For the other supplies, current-sense resistors are integrated into the TPS2343. The current sense thresholds of the 5-V, 3.3-V, 12-V, and −12-V supplies are programmed by one user-supplied resistor connected from MISET to GROUND. The TPS2343 implements slew-rate control using on-chip current sources and user-supplied capacitors. Each supply is controlled by the slew rate capacitor for that supply except for the −12-V supply, which tracks the 12-V supply.

Using the recommended current-sense resistors, current-threshold resistor, and slew-rate control capacitors implements a system with slew rates that meet PCI specifications and can deliver power to any adapter card that meets PCI specifications. If a unique adapter card produces premature current limiting with the recommended programming components, current-limit thresholds can be increased by increasing the value of the resistor connected to MISET or inrush current can be reduced by raising the value of the appropriate slew-rate control capacitors.

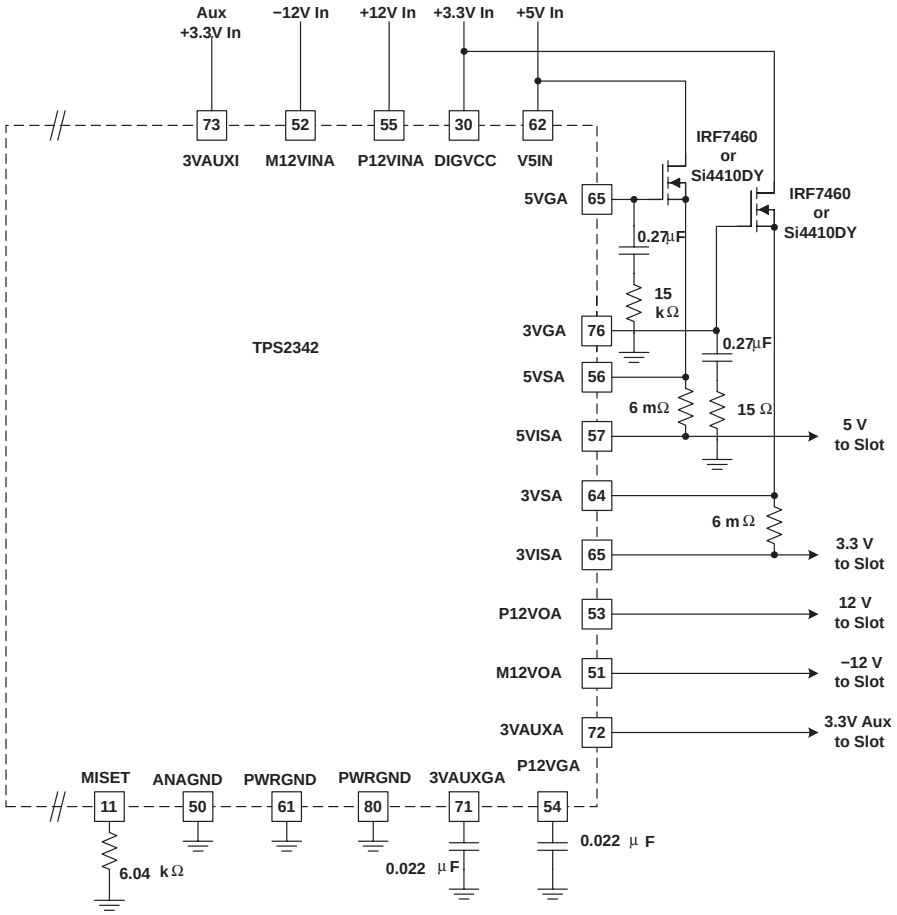


Figure 4. Typical TPS2343 Application Showing Power, Slew-Rate Control and Current-Limit Programming Components (one slot shown)

APPLICATION INFORMATION

Current Regulation and Over Current Protection

In the event of excessively high slot current for the 3.3-V main, 5-V main, or VIO supplies, the TPS2343 regulates load current at the maximum specified current for a fixed 5 ms. If the current does not reduce below the maximum in that time, the TPS2343 shuts down main power to that slot. This minimizes the risk of power rail droop on adjacent slots while at the same time allowing marginal cards to continue to function through brief, high-current demands.

Control of high-current demand is accomplished using closed-loop regulation of the gate voltage, as shown in the block diagram below.

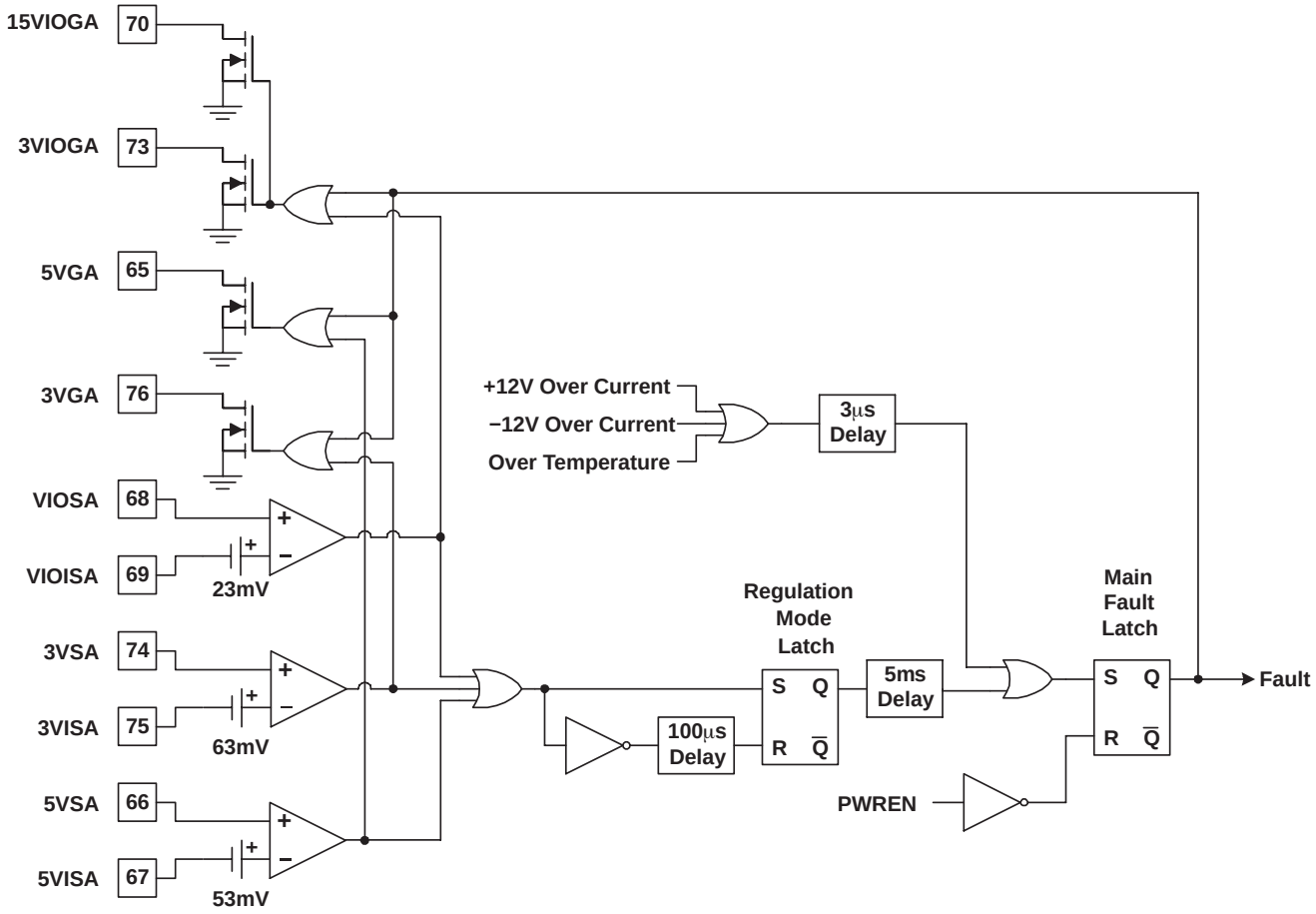


Figure 5. Current Regulation Functional Block Diagram (one slot shown)

Once an overload has been detected on one of these three supplies, the regulation mode latch is set, and gate voltage is reduced. At the same time, a 5-ms timer starts. If the timer elapses without the load current reducing, the main fault latch is set, and the slot latchs off until power is shut off and restarted by the host. If the overload reduces for more than 100 µs, the regulation mode latch clears and the 5-ms timer resets.

For excessively-high slot current on the 12-V main, −12-V main, and 3.3-V auxiliary supplies, the TPS2343 shuts down 3 µs after the fault to prevent disturbance to power on the backplane or damage to the TPS2343.

APPLICATION INFORMATION

VIO Power Selection

PCI−X Local Bus specification revision 2.0 requires that VIO be 3.3 V when the slot is operating in 33-MHz, 66-MHz, or 133-MHz modes and 1.5 V when the slot is operating in 266-MHz or 533-MHz modes. The TPS2343 provides signals to drive external power FETs to select between 3.3 V and 1.5 V for VIO.

To prevent body-diode conduction from the 3.3-V supply to the 1.5-V supply when 3.3 V is delivered to VIO, the 1.5-V VIO switch uses two power FETs in blocking-series connection. To minimize voltage loss, low on-resistance FETs are required (such as IRF1302S or Si4430DY). It is helpful to anticipate the voltage drop in the FETs and adjust the 1.5-V VIO power source for slightly greater than 1.5 V, for example 1.55 V ±25 mV.

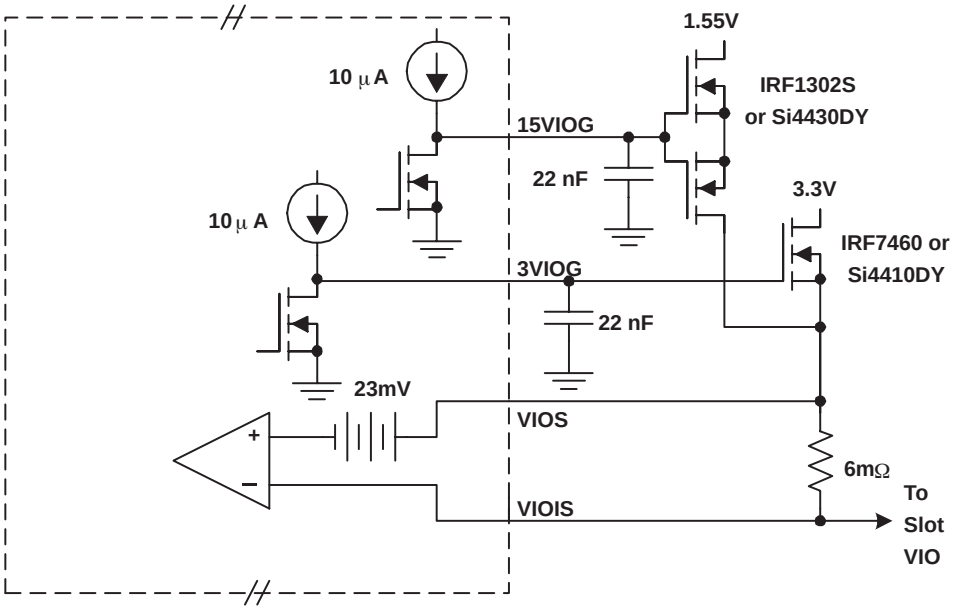


Figure 6. VIO Application Diagram (one slot shown)

When PWREN is asserted, depending on VIOSEL, either 15VIOG or 3VIOG ramps up concurrently with the other main power supplies. When PWREN is deasserted, 15VIOG or 3VIOG ramps down concurrently with the other main power supplies.

Gate slewing caps are used on the VIO channels. One cap is used for the 3VIOGx and another for the 15VIOGx in order to set the slew rate properly for a 1.5-V or 3.3-V channel. There is only one charging current on VIO which is set at 10 μA and switched between the two pins depending on the VIOSELx input.

PCI specifications limit adapter card VIO capacitance to 150 μF. It is recommended that the backplane also have between 10 μF and 50 μF of bypass capacitance on VIO to minimize transients. The capacitance on each gate is 22 nF, producing a gate slew rate of approximately 0.45 V/ms. The averagelimits VIO capacitive inrush current is approximately 68 mA.

APPLICATION INFORMATION

Digital Communications

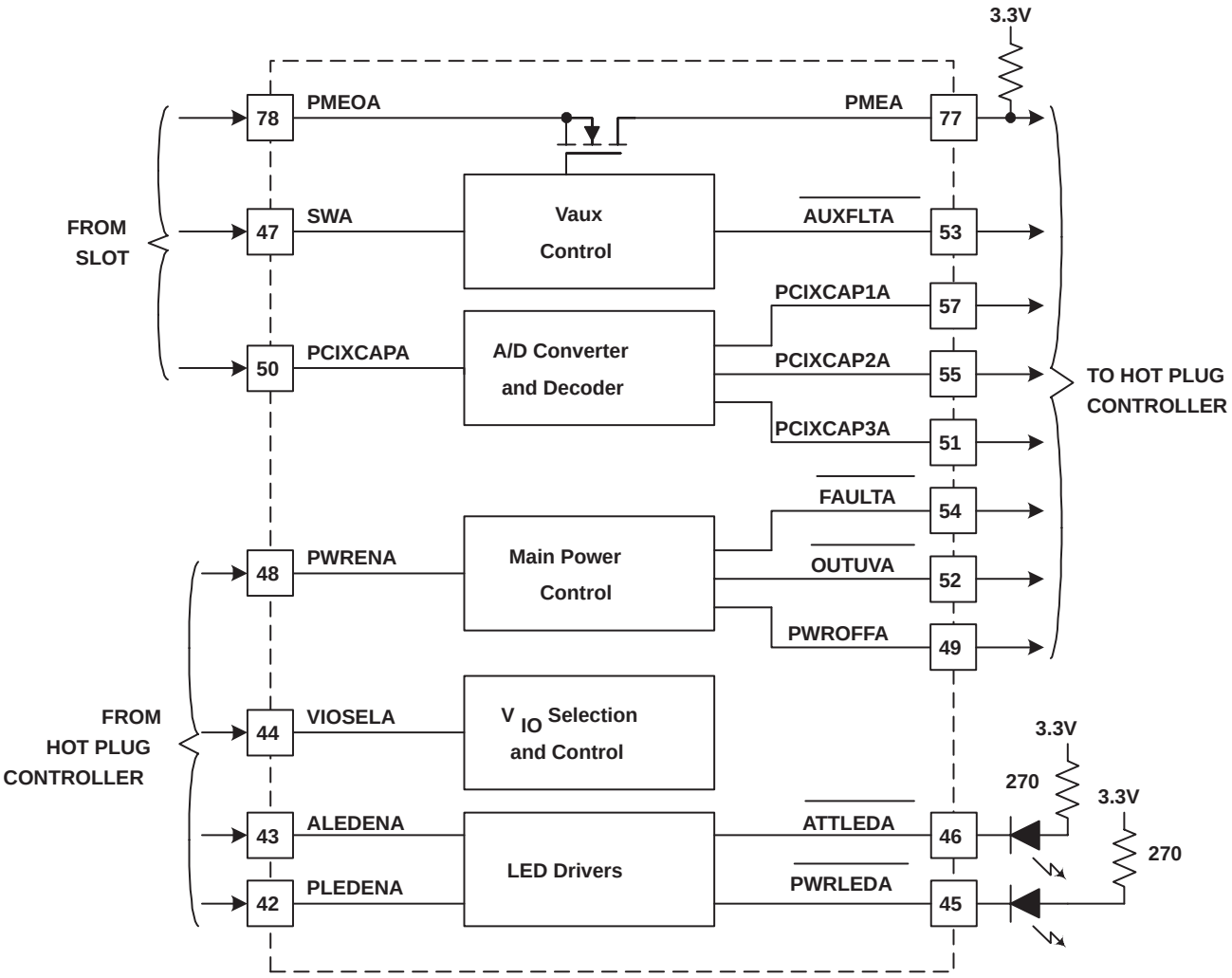
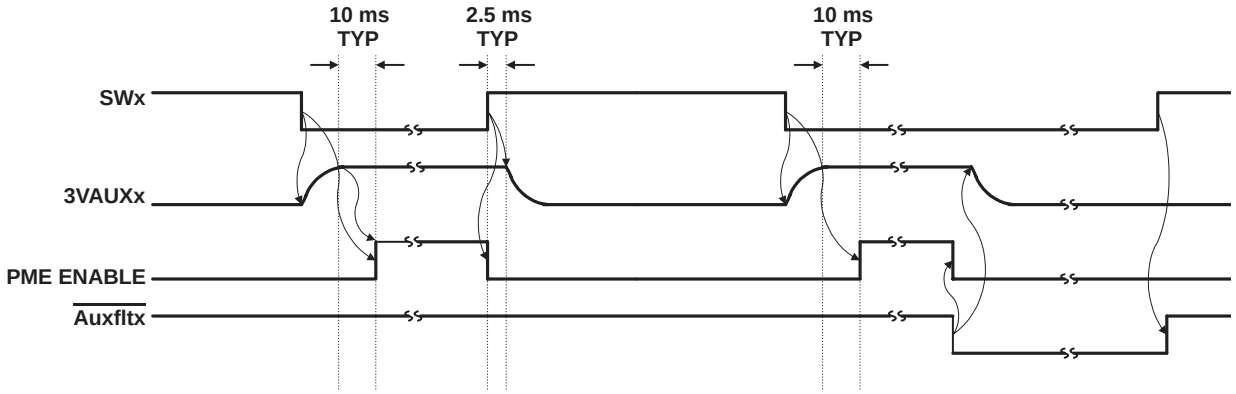


Figure 7. Digital Interface Application Diagram (one slot shown)

APPLICATION INFORMATION

Power Cycling and $\overline{PME}$

The PCI power management specification defines a signal called $\overline{PME}$ (power management event) to allow requests for power state changes to be communicated from the slot back to the system. The TPS2343 provides a slot-specific $\overline{PMEx}$ input and a gated $\overline{PMEOx}$ output that can be monitored by the system. The gated $\overline{PMEOx}$ output is enabled a delay after the SWx slot switch closes (SWx low) as shown in the timing diagram below. The purpose of the delay is to ensure that 3.3-V_{AUX} power is stable to the slot before connecting $\overline{PMEx}$ the signal. If the $\overline{PMEx}$ signal was presented to the system while 3.3-V_{AUX} power was still ramping up, a false trigger could result.The 3.3-V_{AUX} circuitry provides over current fault detection. In the event of an over current fault on V_{AUX}, the slot 3.3-V_{AUX} and $\overline{PME}$ signals are immediately disconnected. The fault state is latched internally in the TPS2343 and is cleared either by opening the SWx slot switch or by removing the 3.3-V_{AUX} power to the TPS2343.

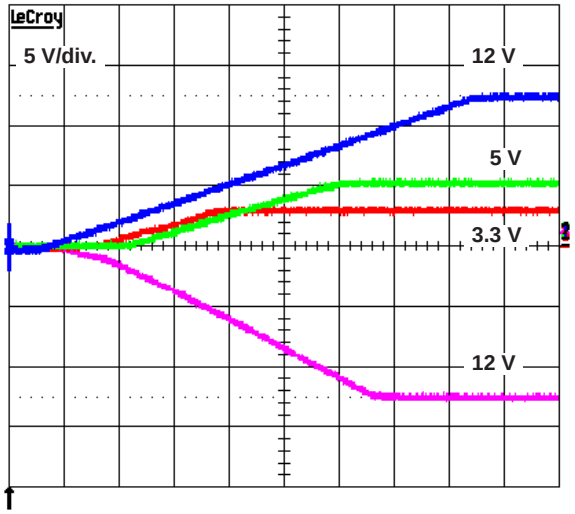


V_{AUX} and PME Gating

When SWx is closed (low), 3VAUXx power is immediately applied to the slot with controlled slew rate, minimizing inrush current into 3VAUXx bypass capacitors. After 3VAUXx power completes ramping up, a delay timer starts. At the end of the delay timer cycle, the $\overline{PMEx}$ enable switches close, allowing connection of the $\overline{PMEx}$ signal to the $\overline{PMEOx}$ output. Multiple $\overline{PMEOx}$ output pins can be connected to the same node, creating a $\overline{PME}$ bus that can be connected to a master system interrupt input.When SWx is opened (high) or if there is a power fault on slot x, the $\overline{PMEx}$ enable switch for that slot is immediately opened and the 3VAUXx power for that slot is removed. Although these events happen at approximately the same time, the 3VAUXx power should remain high until the $\overline{PMEx}$ switch is open so that falling 3VAUXx power does not cause a nuisance $\overline{PMEx}$ interrupt. To insure that 3VAUXx remains high during a power fault, 3VAUXx should have a bypass capacitance of at least 20 µF. If the capacitor is not available on the inserted card, it should be provided on the system board.The PME circuit operates independently of any of the main power supplies.

TYPICAL CHARACTERISTICS

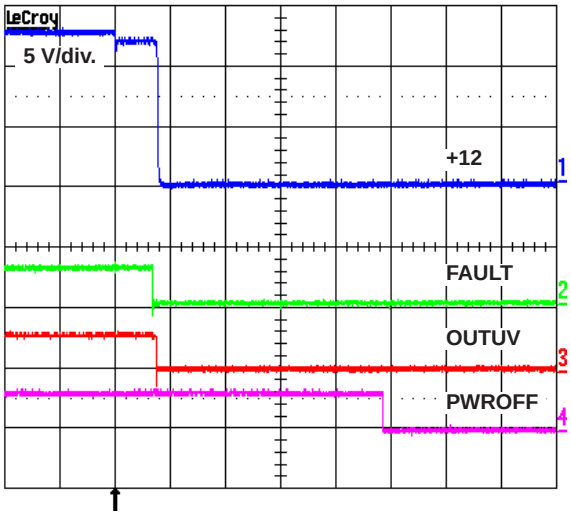
SLOT VOLTAGE TURN ON FROM PWREN



t − Time − 5 ms/div.

Figure 8

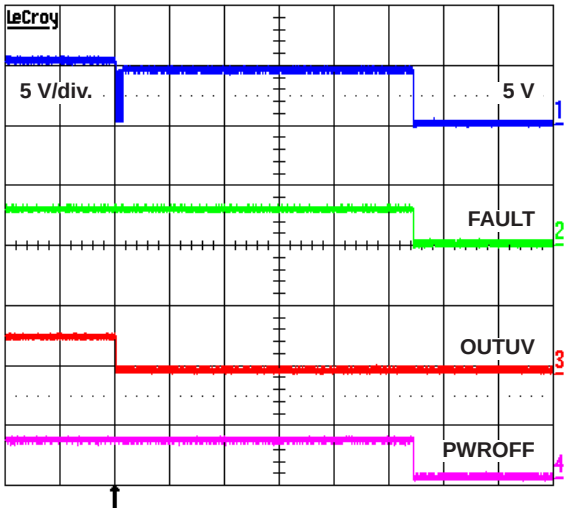
TURN OFF FROM 12 V OVERCURRENT



t − Time − 5 μs/div.

Figure 9

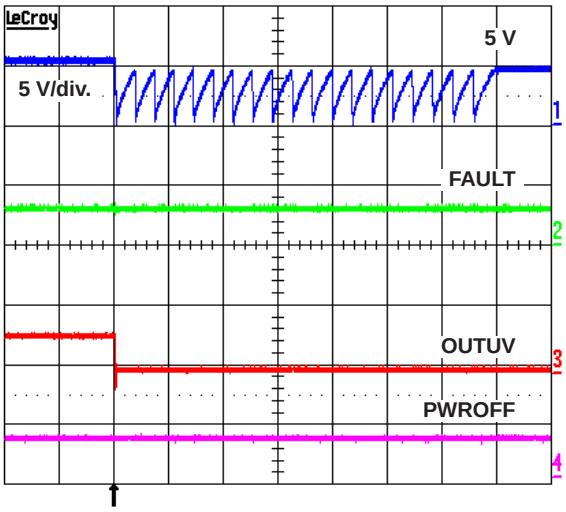
5 V TURN OFF FOR 5 V OVERCURRENT



t − Time − 1 ms/div.

Figure 10

5 V AT COARSE REGULATION ON 5 V OVERCURRENT

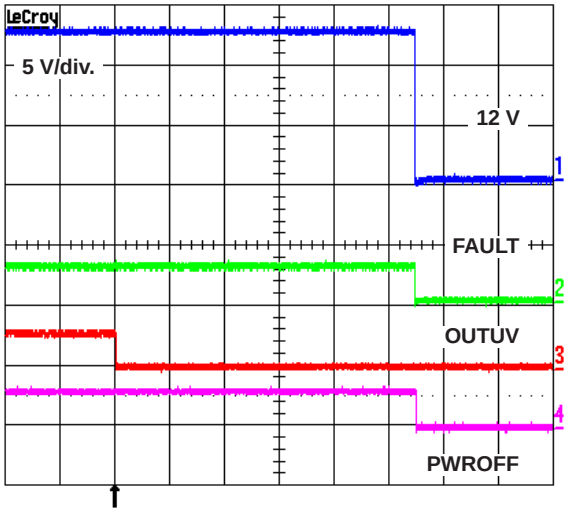


t − Time − 20 μs/div.

Figure 11

TYPICAL CHARACTERISTICS

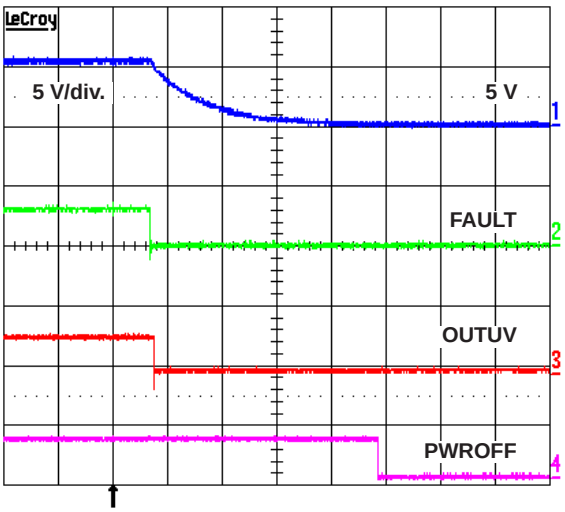
12 V TURN OFF FOR 5 V OVERCURRENT



t − Time − 1 ms/div.

Figure 12

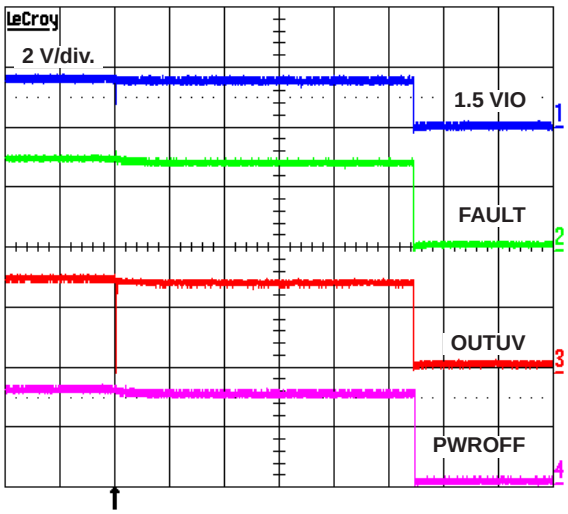
5 V TURN OFF FOR 12 V OVERCURRENT



t − Time − 5 μs/div.

Figure 13

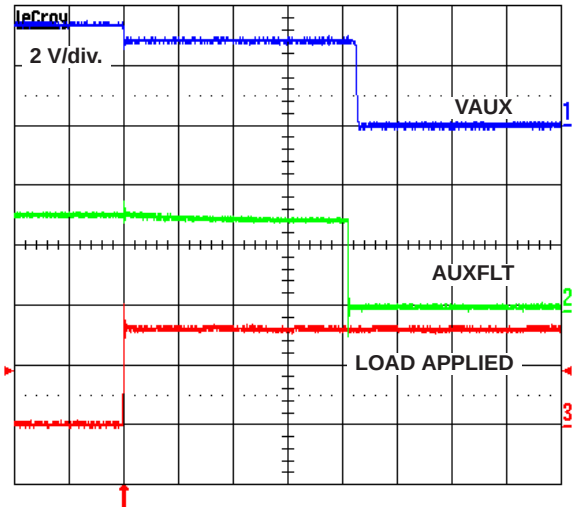
1.5 V FOR VIO OVERCURRENT



t − Time − 1 ms/div.

Figure 14

VAUX FOR VAUX OVERCURRENT

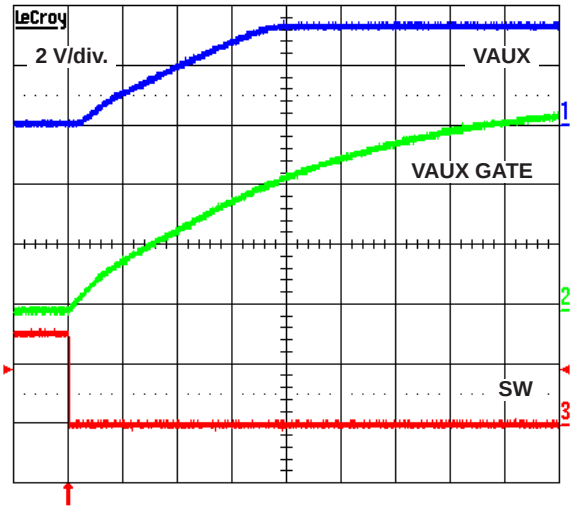


t − Time − 5 μs/div.

Figure 15

TYPICAL CHARACTERISTICS

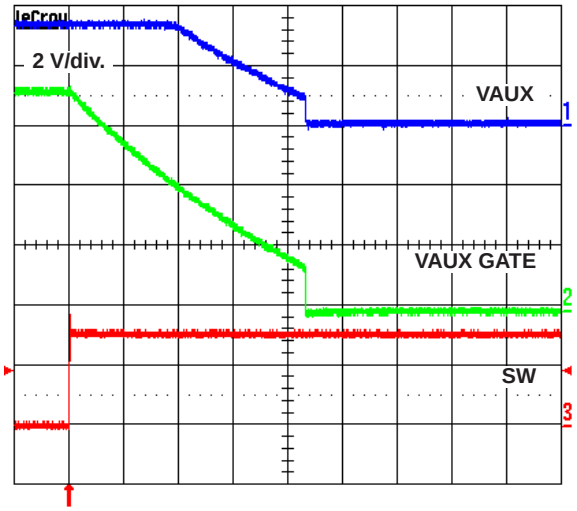
VAUX ON FROM SW



t − Time − 2 ms/div.

Figure 16

VAUX OFF FROM SW



t − Time − 0.1 ms/div.

Figure 17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2343DDP	OBSOLETE	HTSSOP	DDP	80		TBD	Call TI	Call TI	-40 to 85	TPS2343DDP	
TPS2343DDPG3	OBSOLETE	HTSSOP	DDP	80		TBD	Call TI	Call TI	-40 to 85	TPS2343DDP	
TPS2343DDPR	OBSOLETE	HTSSOP	DDP	80		TBD	Call TI	Call TI	-40 to 85	TPS2343DDP	

(1) The marketing status values are defined as follows:
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(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

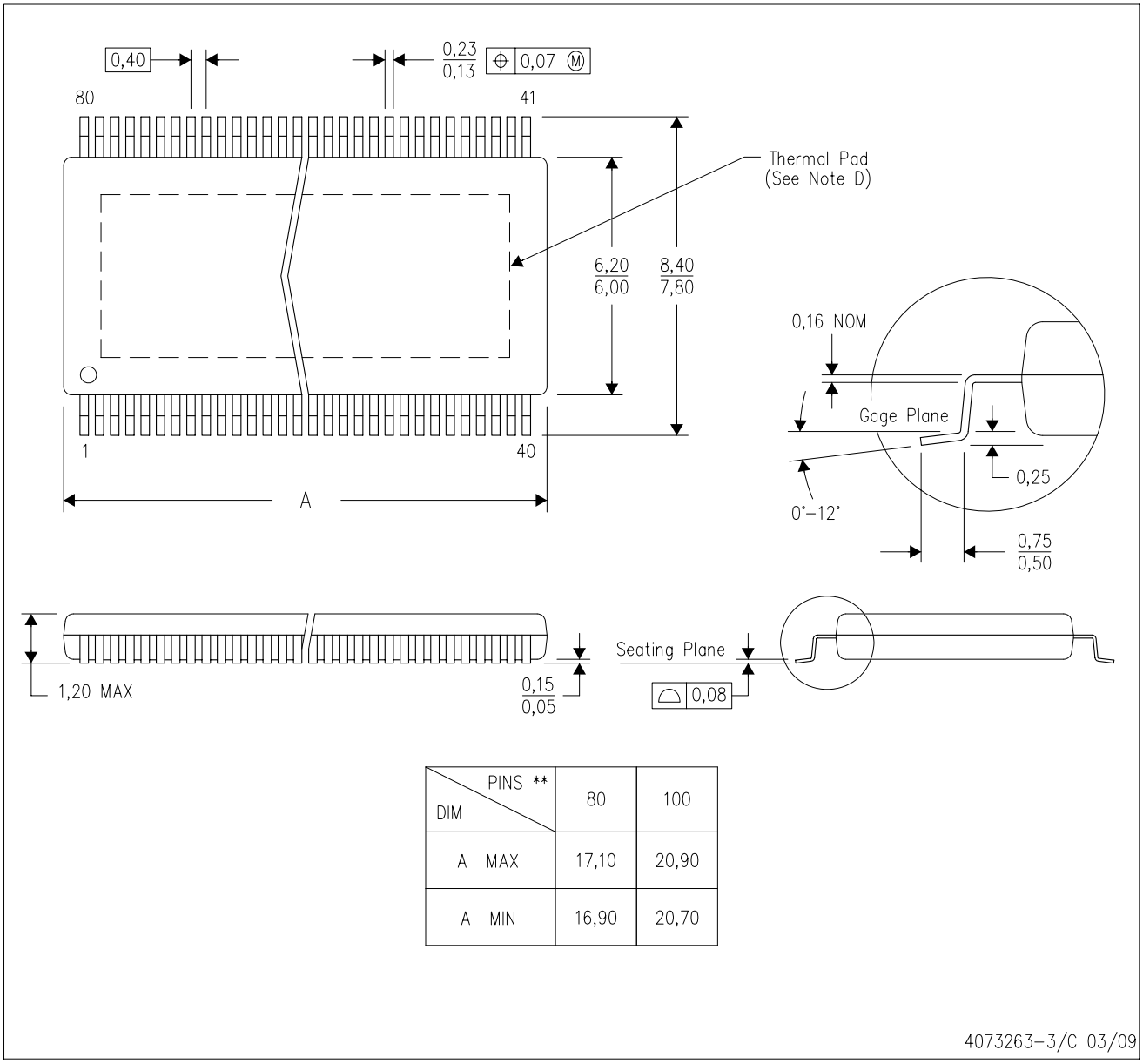
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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80–PIN SHOWN



DIM \ PINS **	80	100
A MAX	17,10	20,90
A MIN	16,90	20,70

4073263–3/C 03/09

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

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